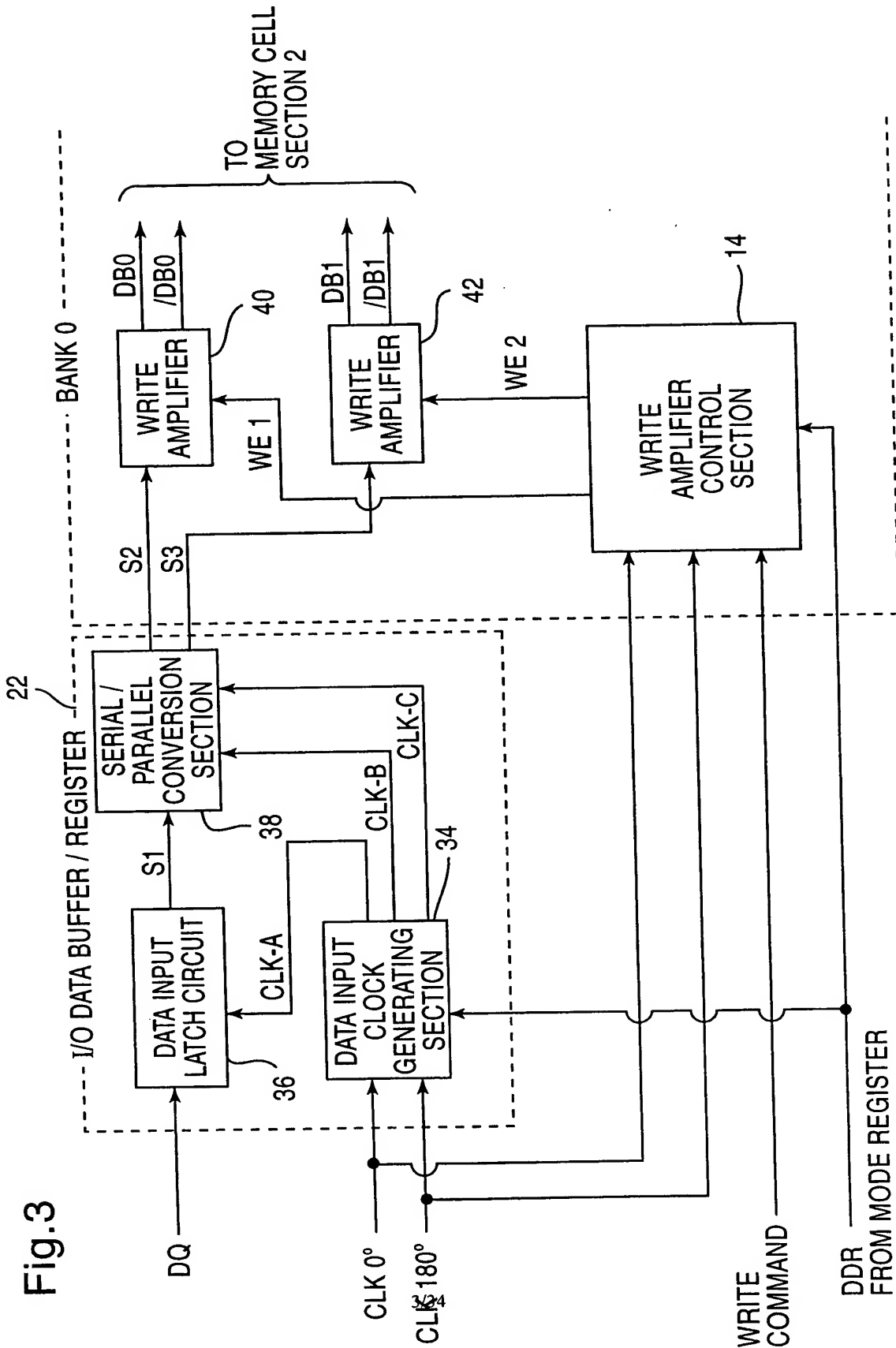


Fig.2

COMMAND FUNCTION NAME	COMMAND	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	A11	A10	A9 ~ A0
		n-1	n							
NON-SELECTION OF DEVICE	DESL	H	X	H	X	X	X	X	X	X
NO OPERATION	NOP	H	X	L	H	H	H	X	X	X
READ	READ	H	X	L	H	L	H	V	L	V
READ / AUTO PRECHARGE	READA	H	X	L	H	L	H	V	H	V
WRITE	WRIT	H	X	L	H	L	L	V	L	V
WRITE / AUTO PRECHARGE	WRITA	H	X	L	H	L	L	V	H	V
BANK ACTIVE (RAS)	ACTV	H	X	L	L	H	H	V	V	V
SINGLE BANK PRECHARGE	PRE	H	X	L	L	H	L	V	L	X
ALL BANK PRECHARGE	PALL	H	X	L	L	H	L	X	H	X
MODE REGISTER SET	MRS	H	X	L	L	L	L	L	V	V



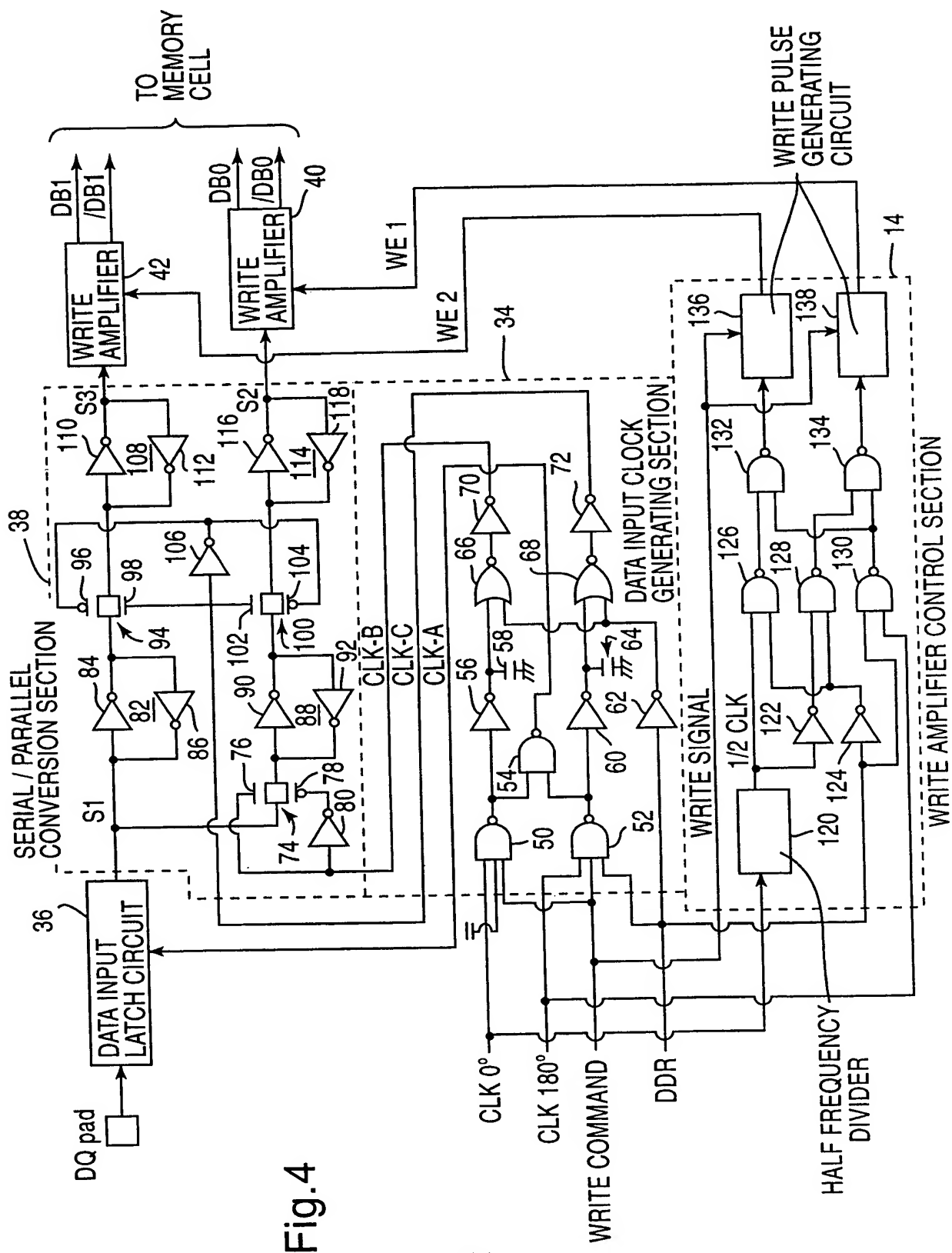


Fig. 4

Fig.5

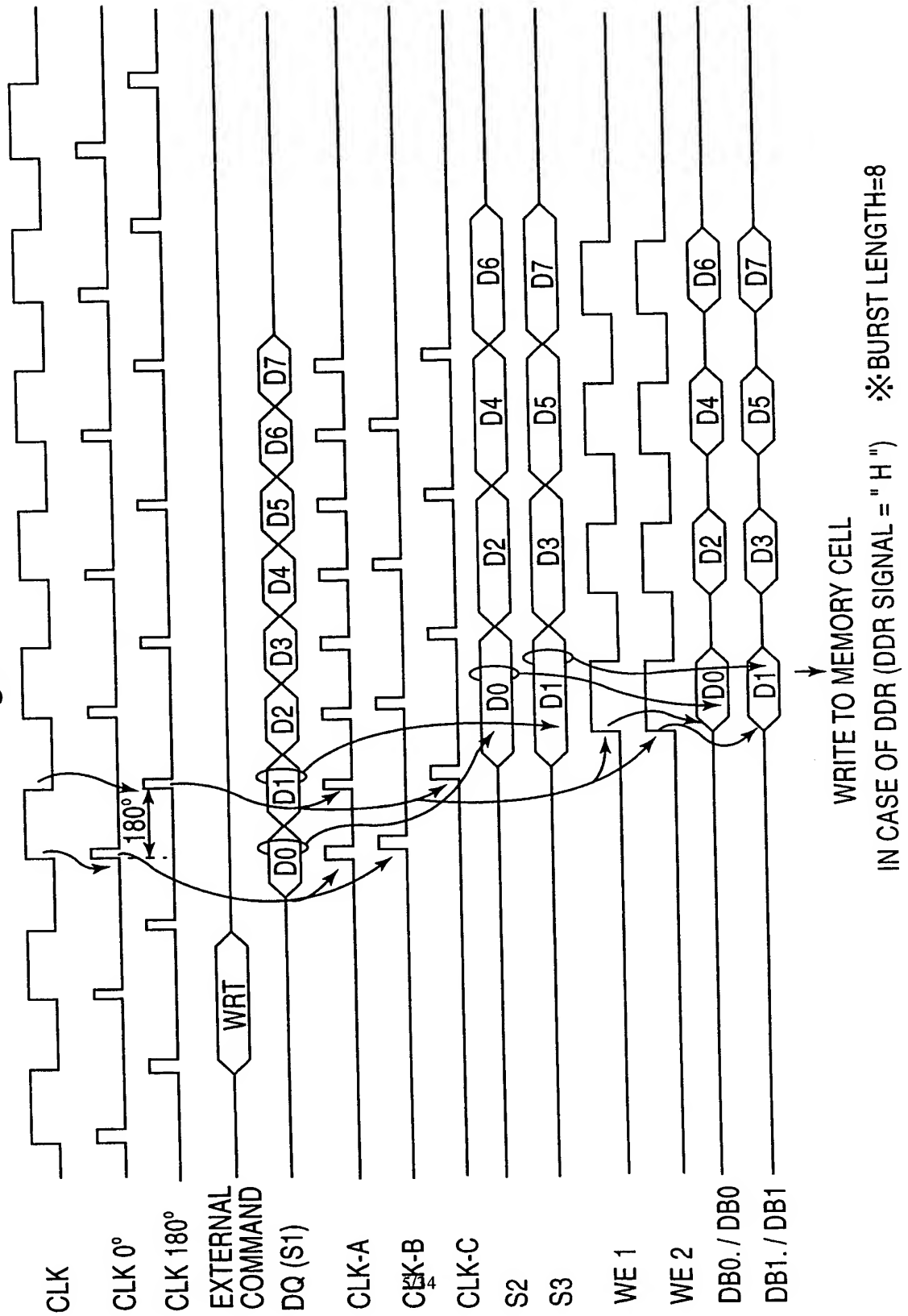
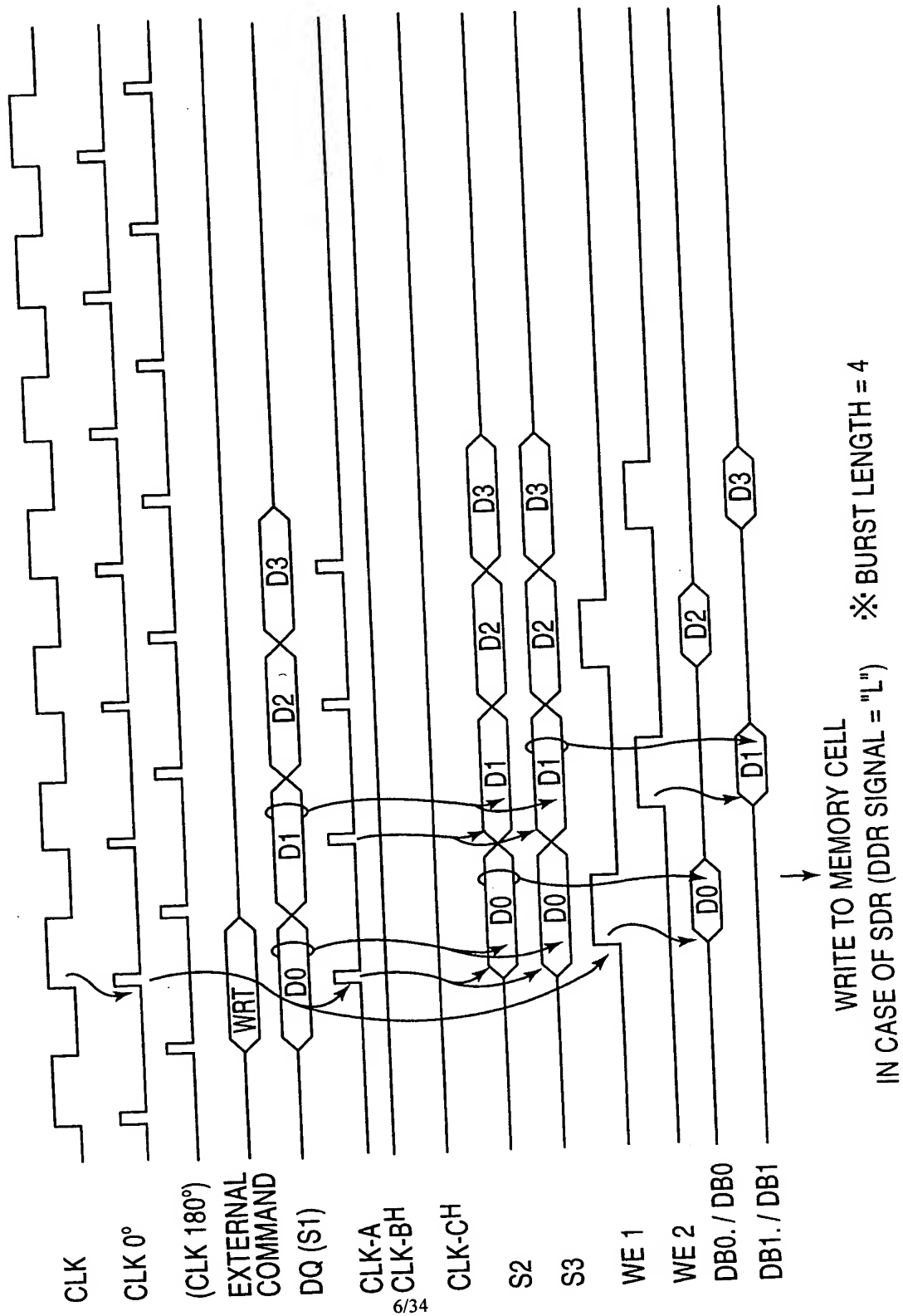


Fig. 6



16



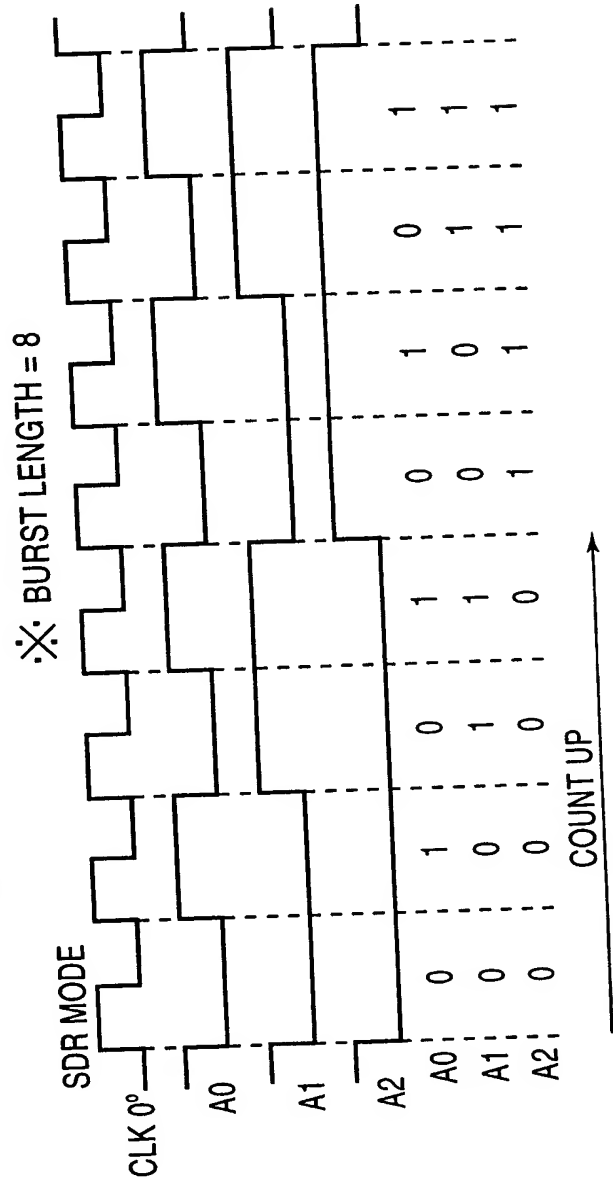
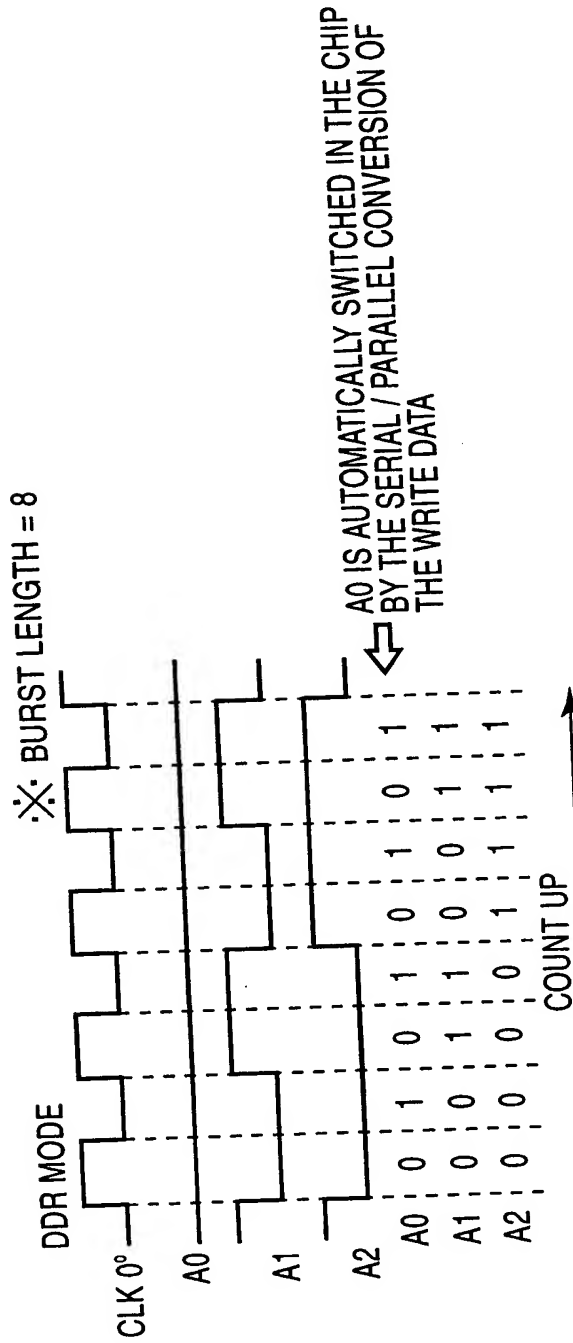


Fig. 9

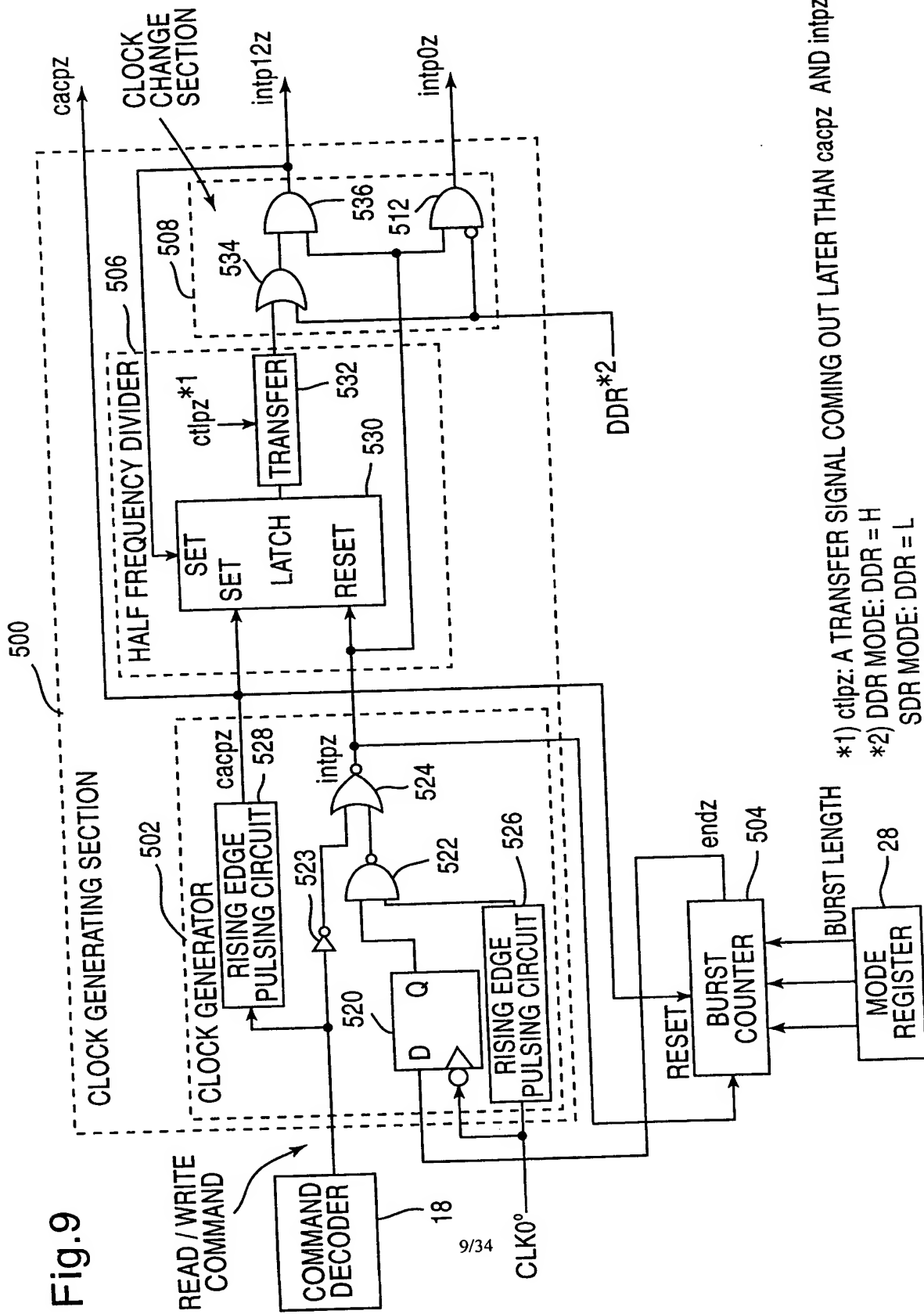


Fig.10

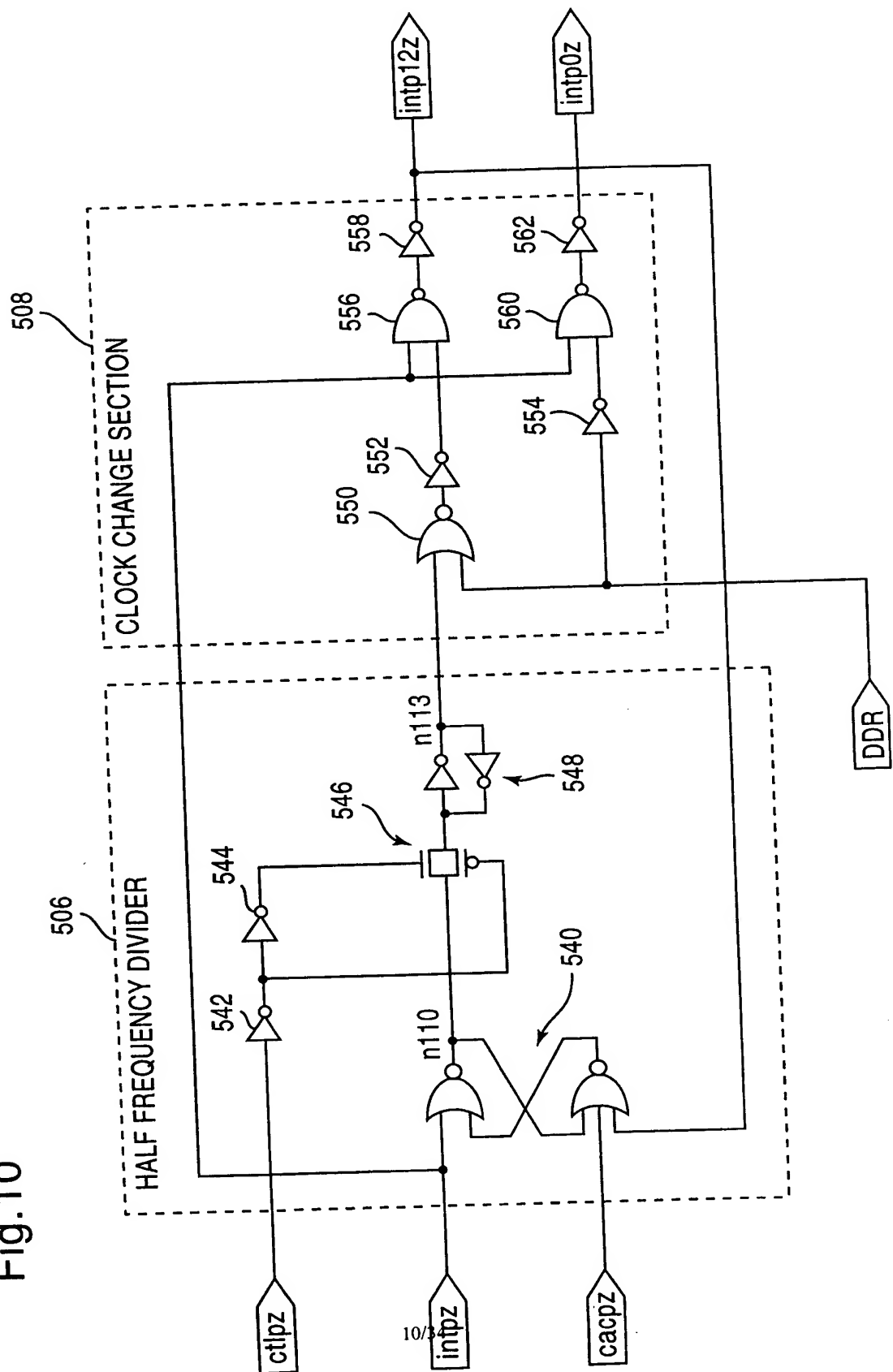


Fig.11

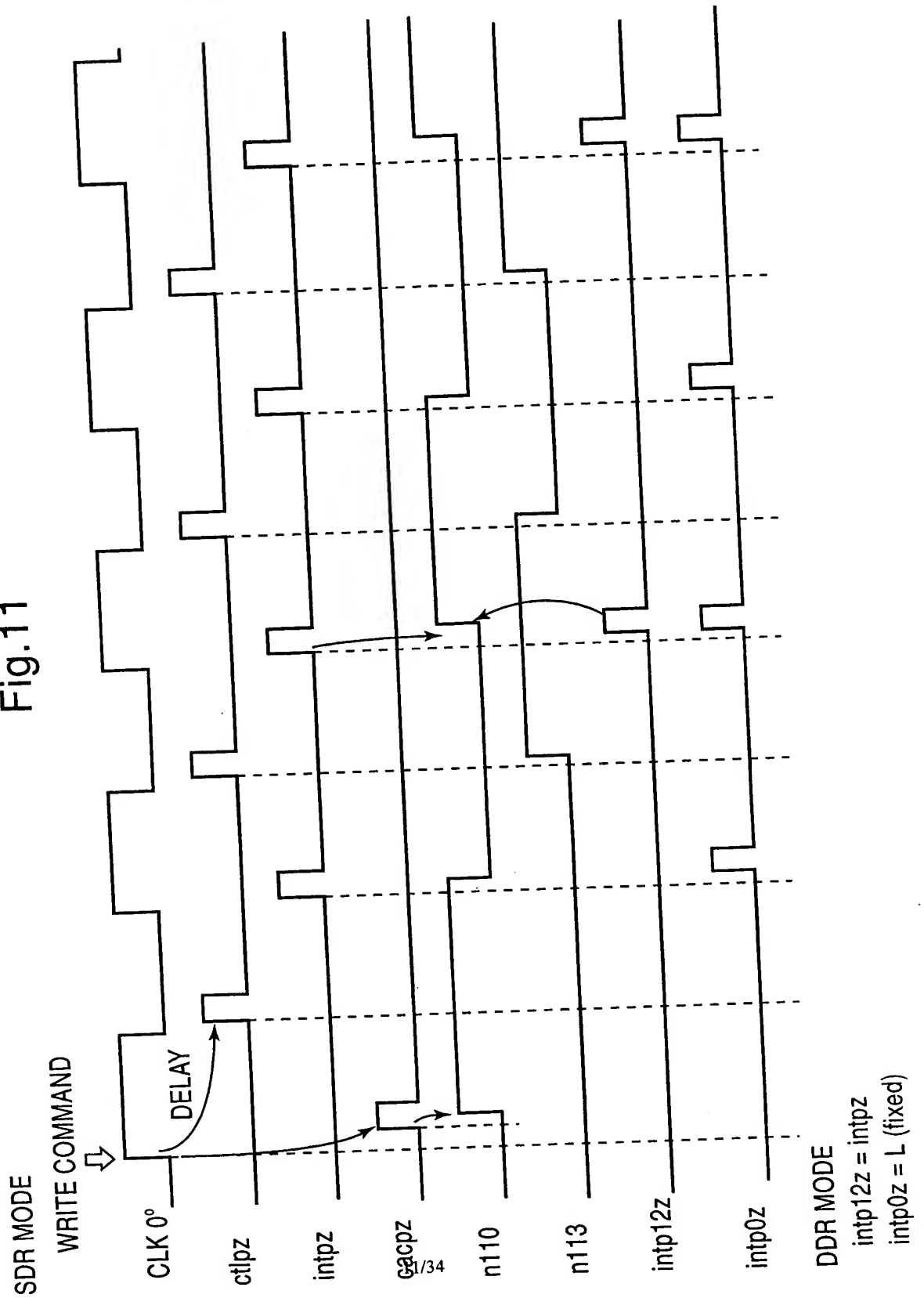
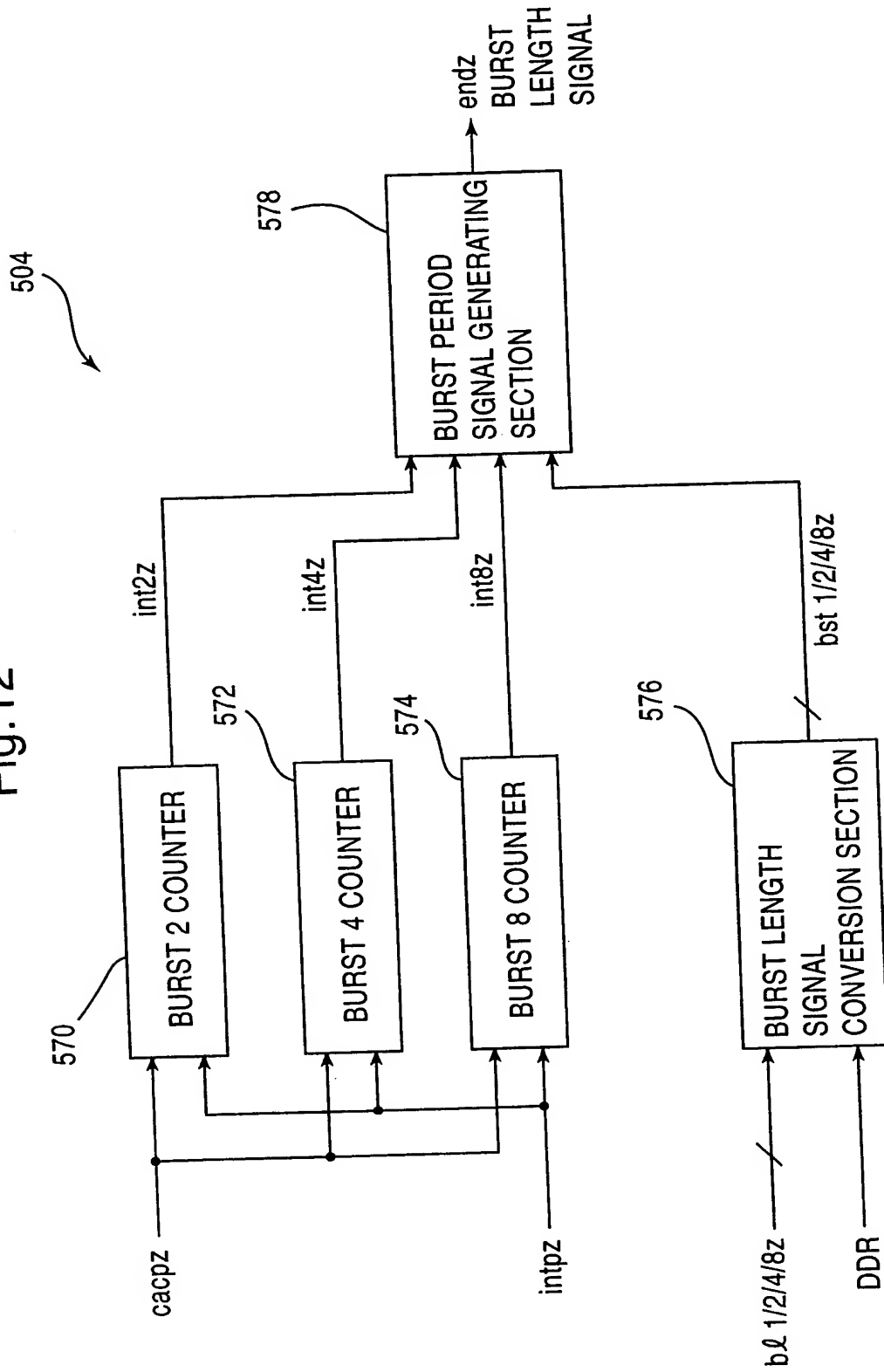


Fig.12



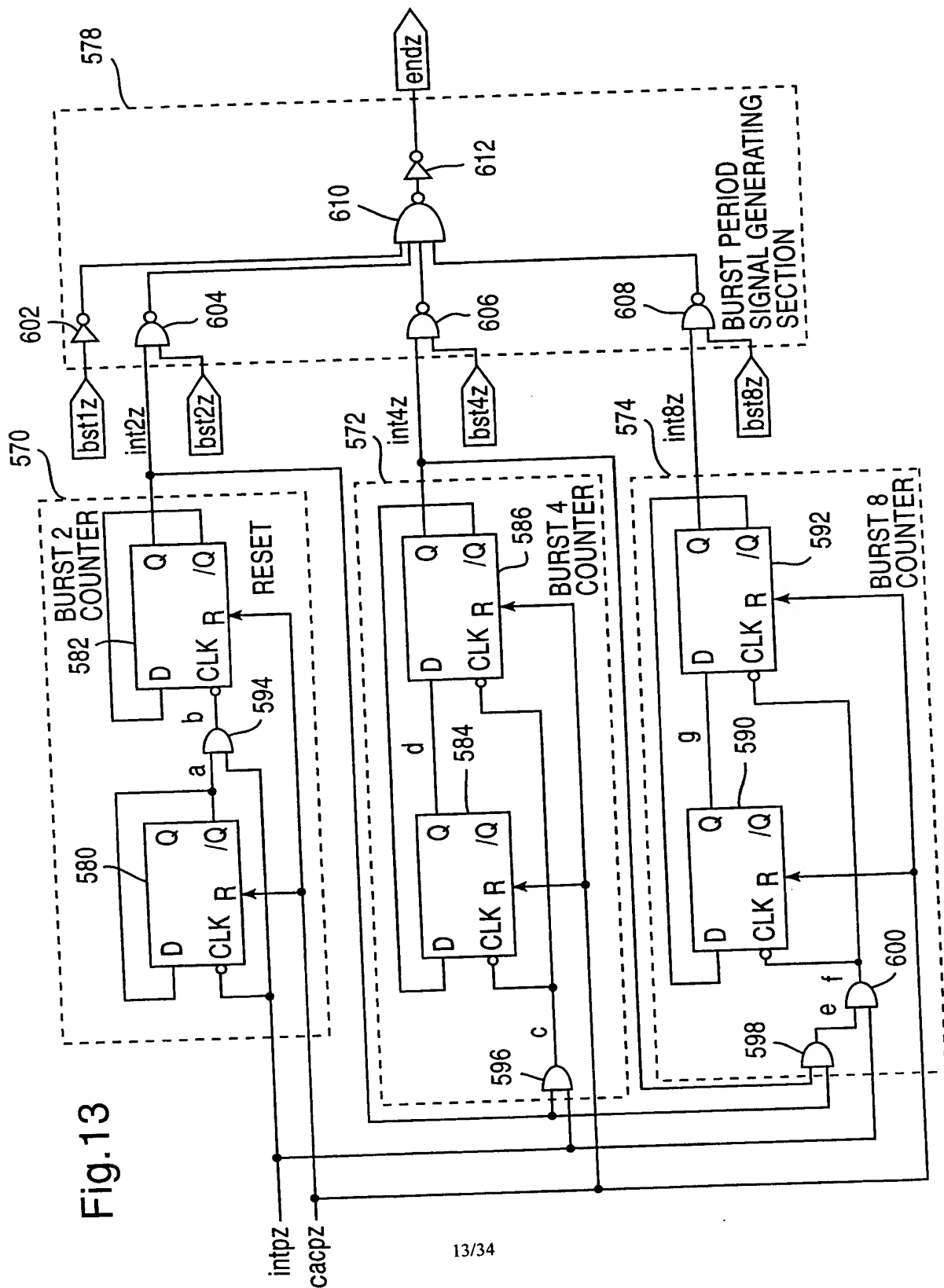


Fig. 13

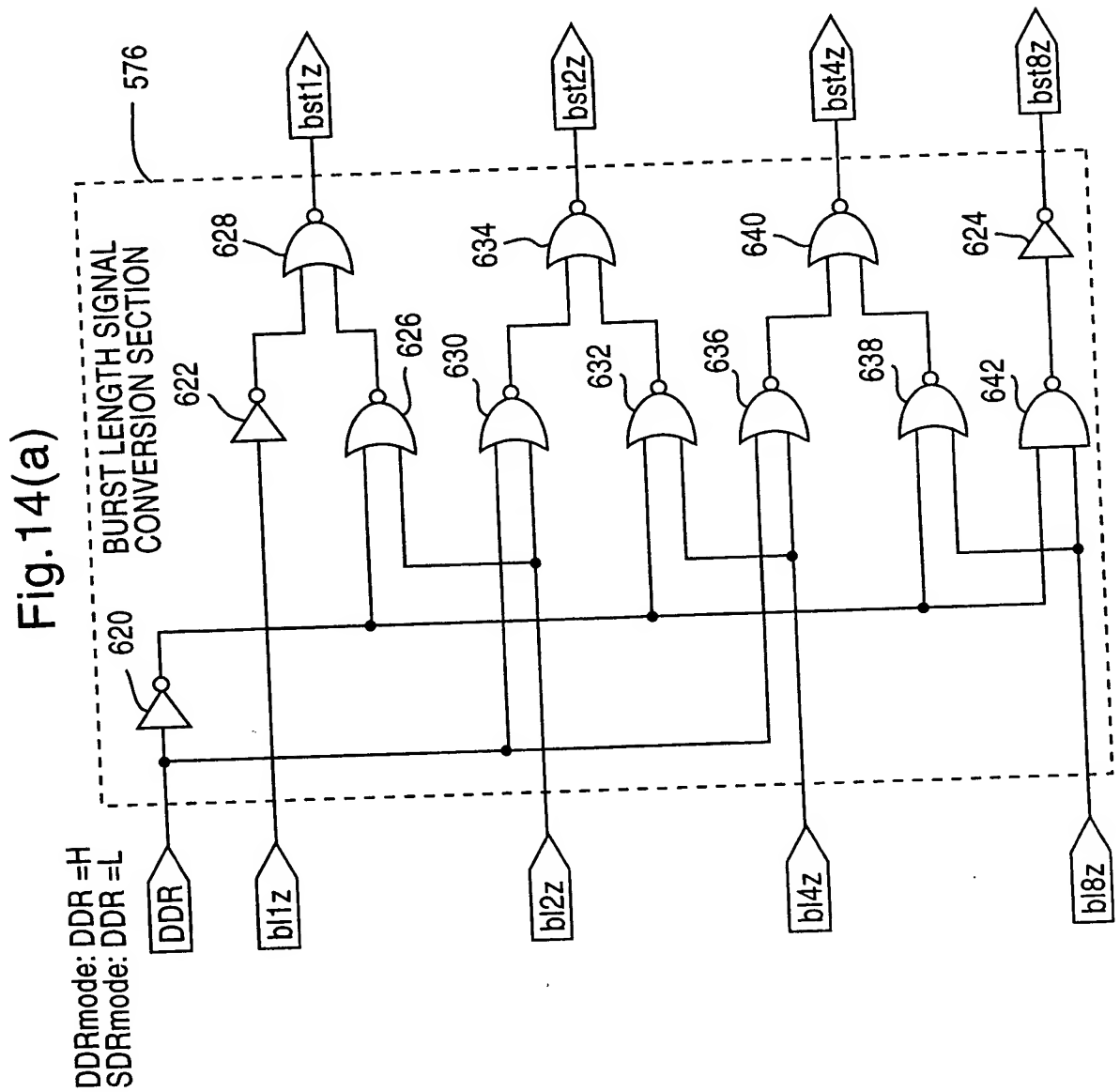
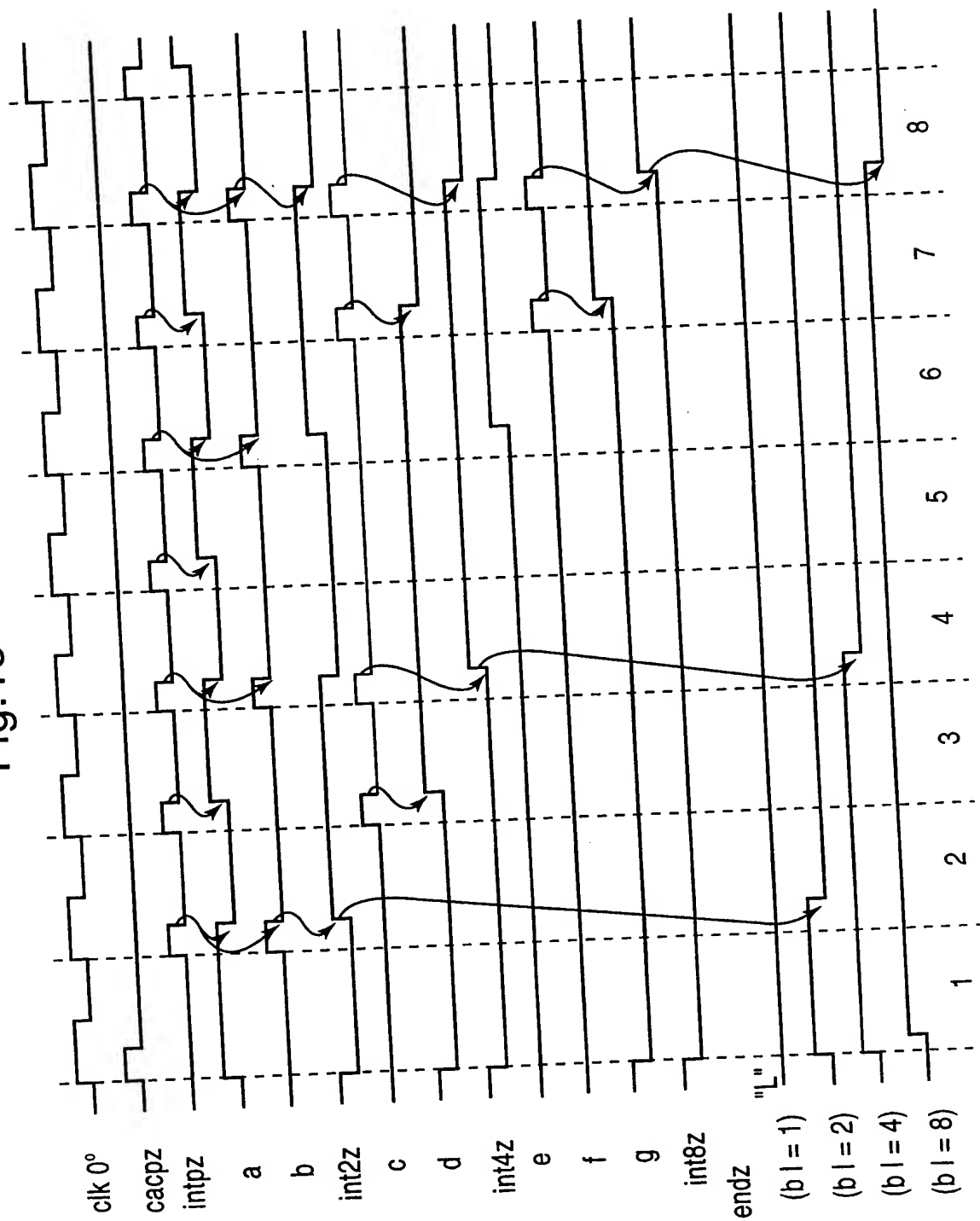


Fig. 14(b)

	DDRmode	SDRmode
bst1z	b12z	b11z
bst2z	b14z	b12z
bst4z	b18z	b14z
bst8z	L	b18z

Fig.15



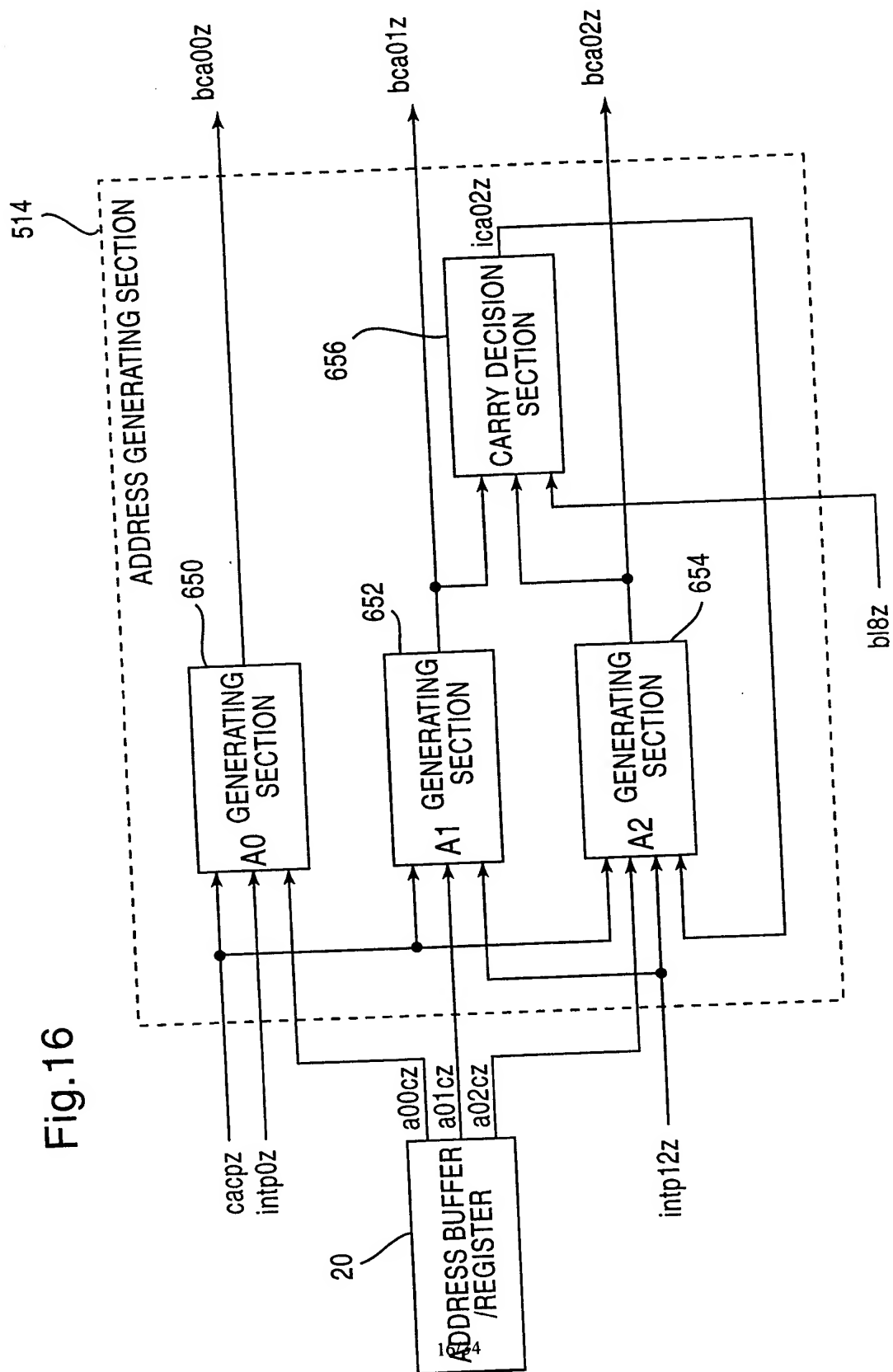


Fig.16

Fig. 17

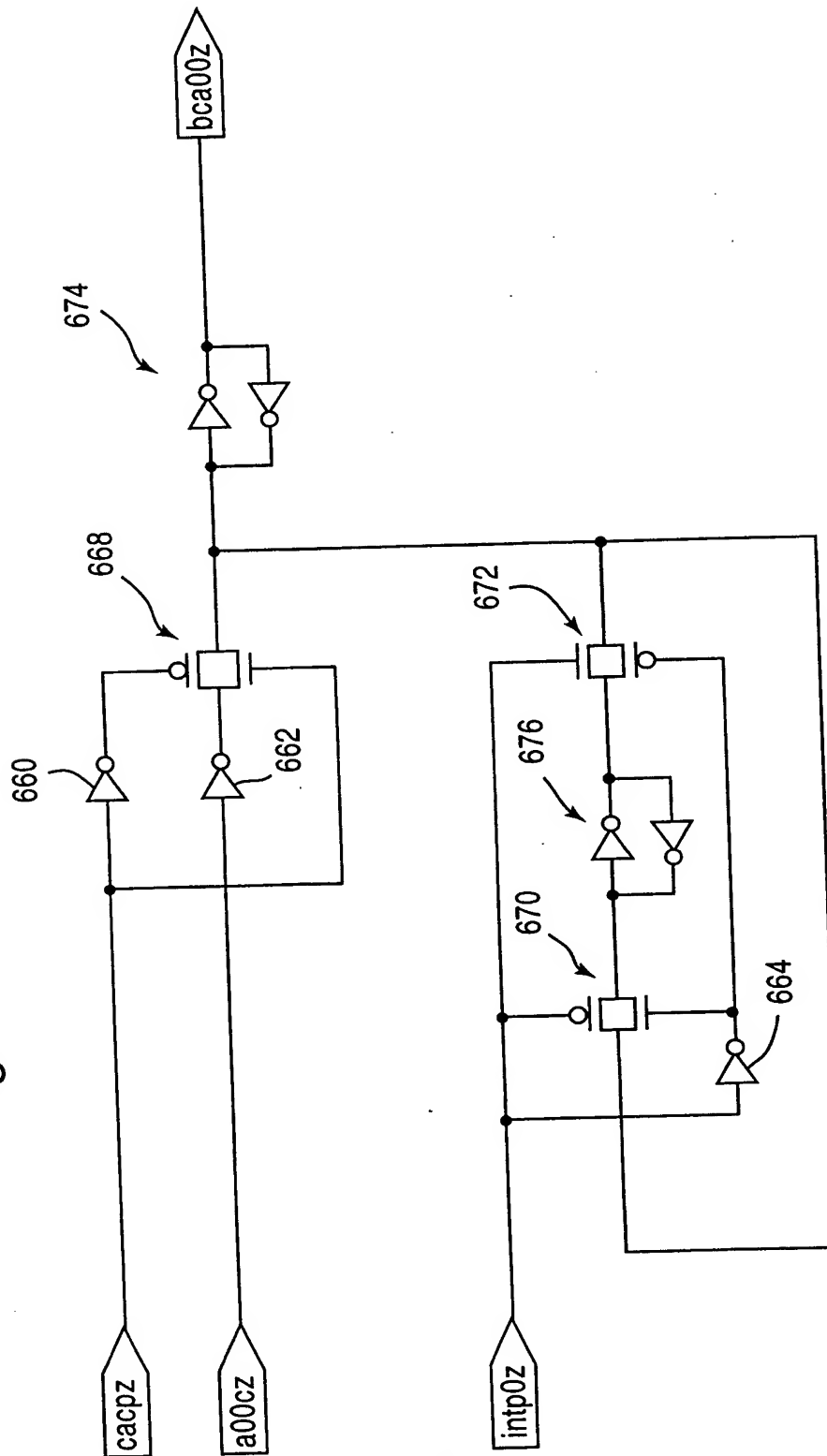


Fig.18

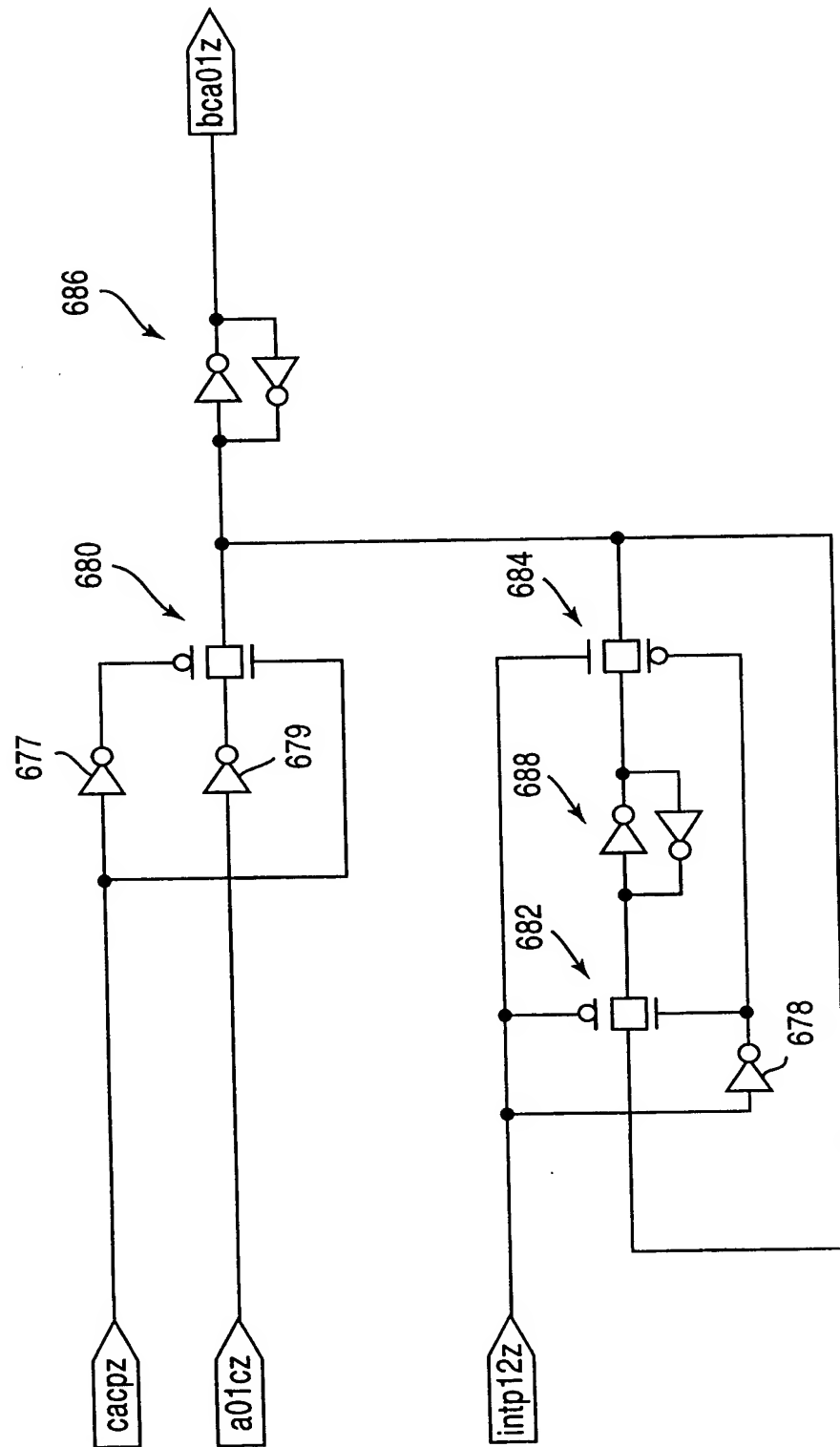


Fig.19

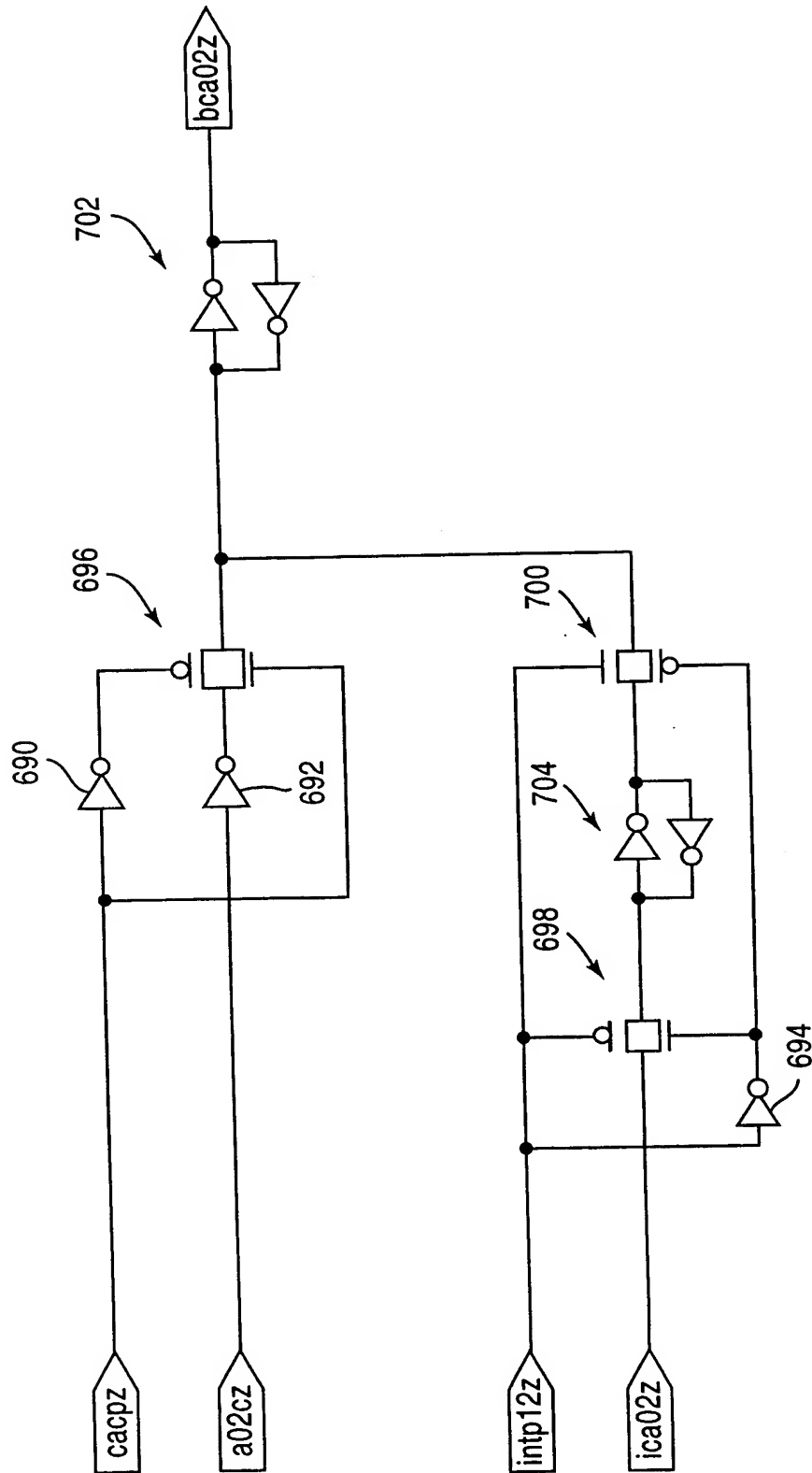
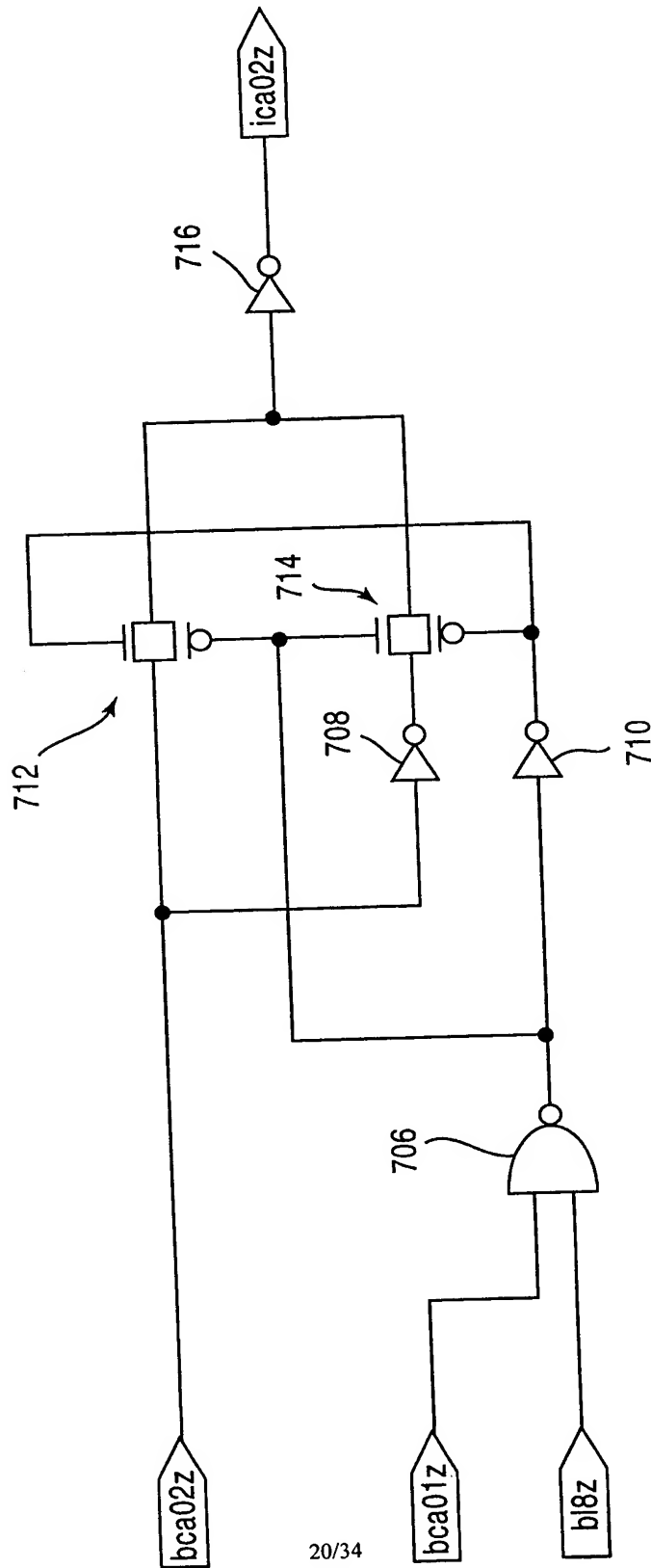


Fig.20



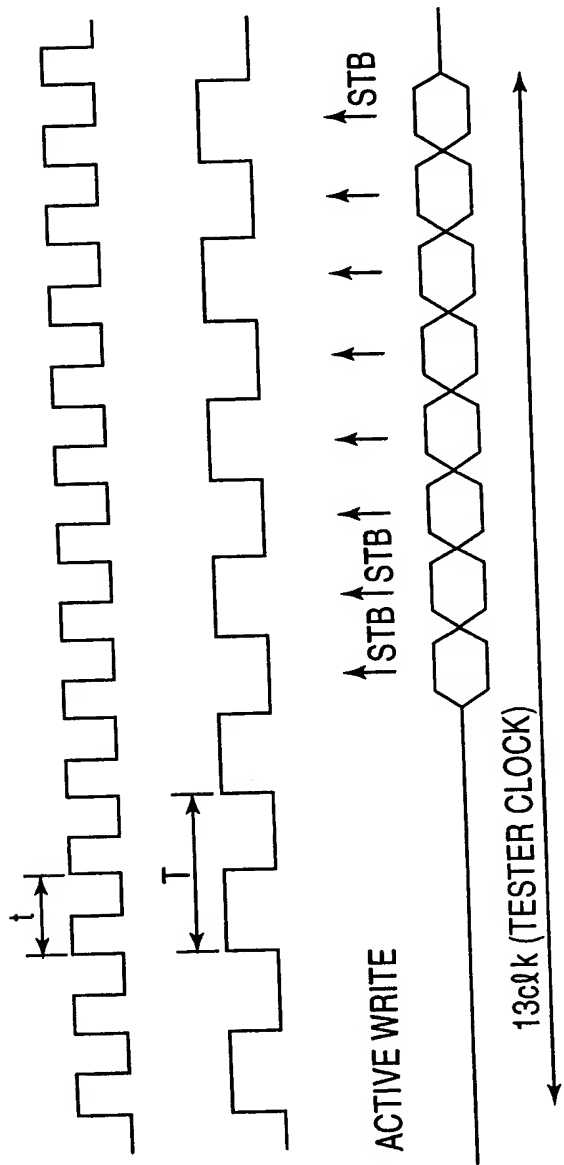


Fig. 21(a)

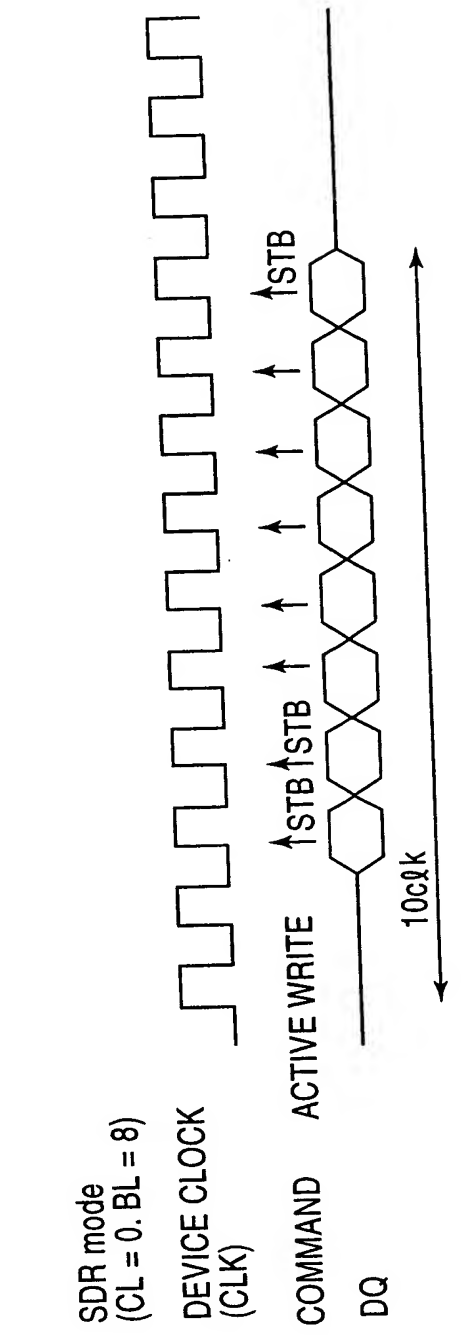


Fig. 21(b)

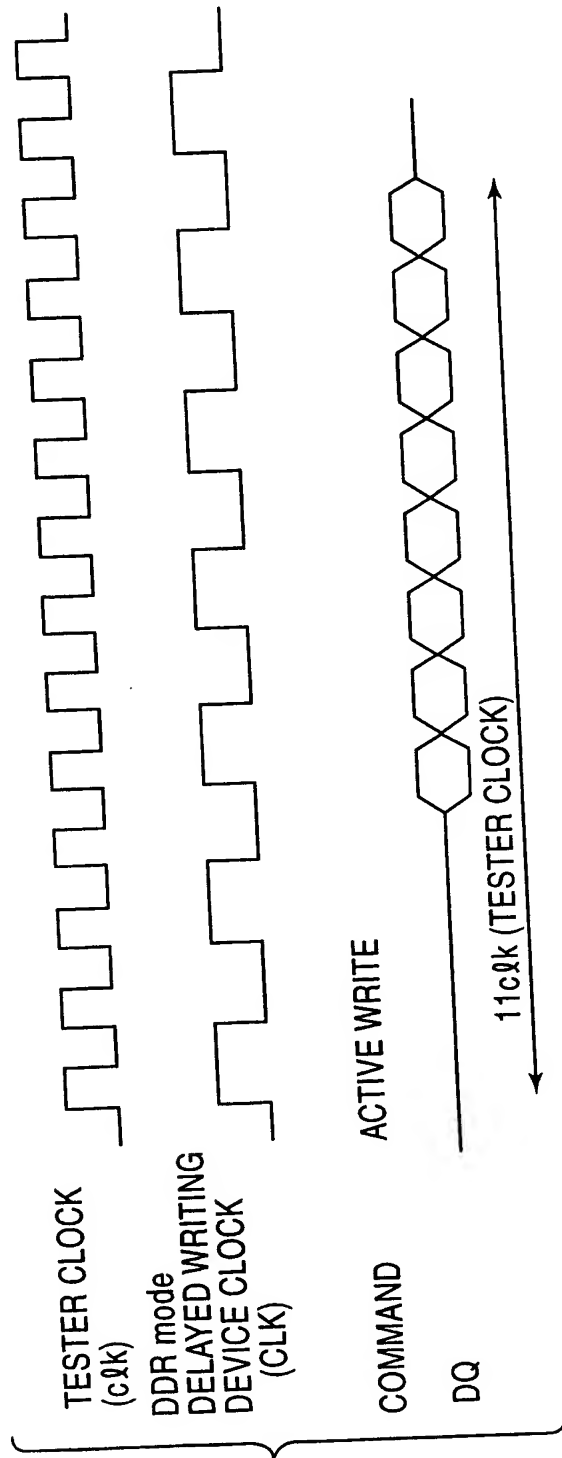


Fig. 22(a)

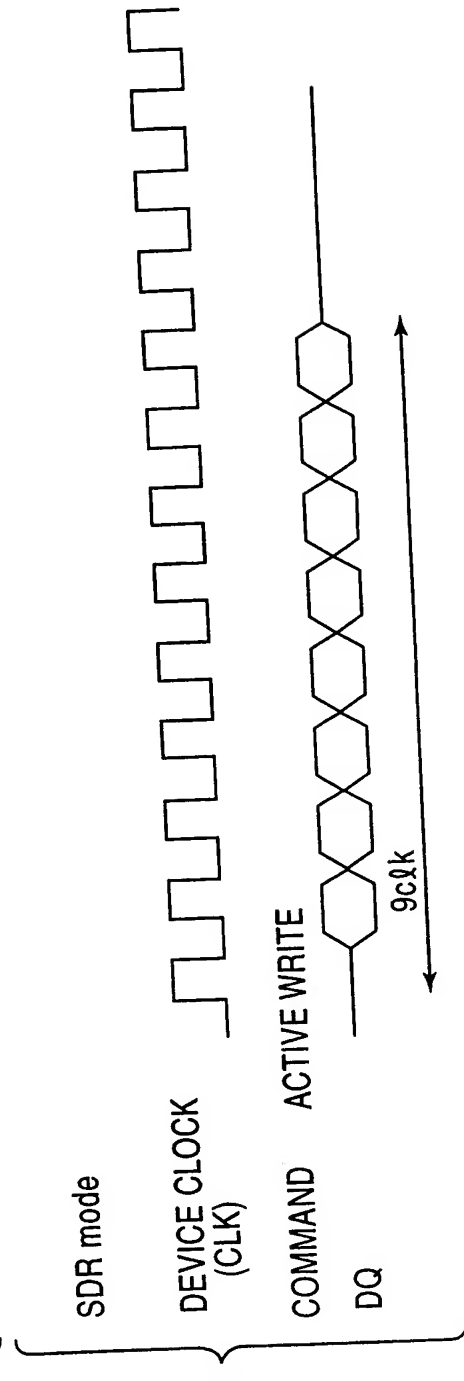


Fig. 22(b)

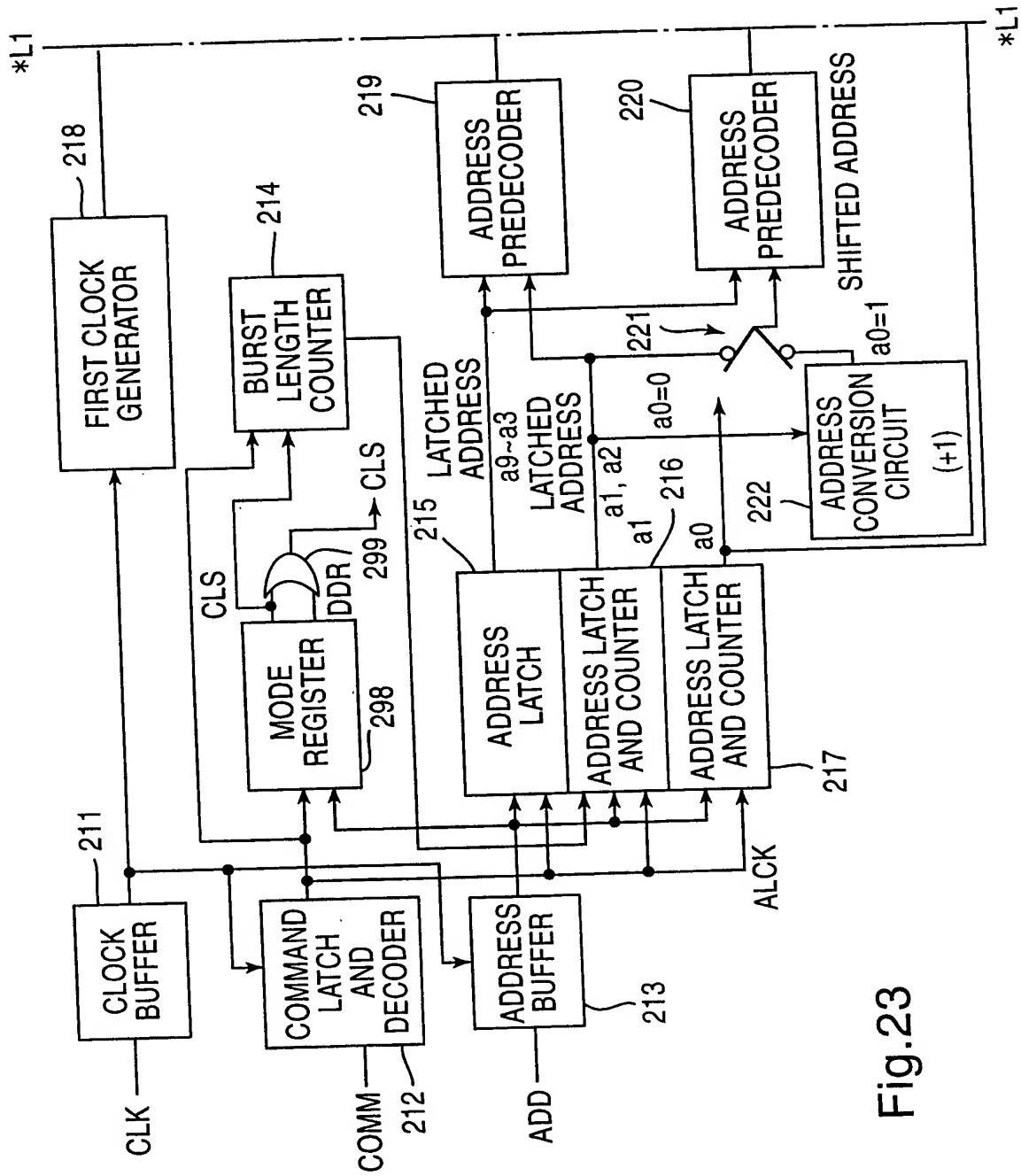


Fig.23

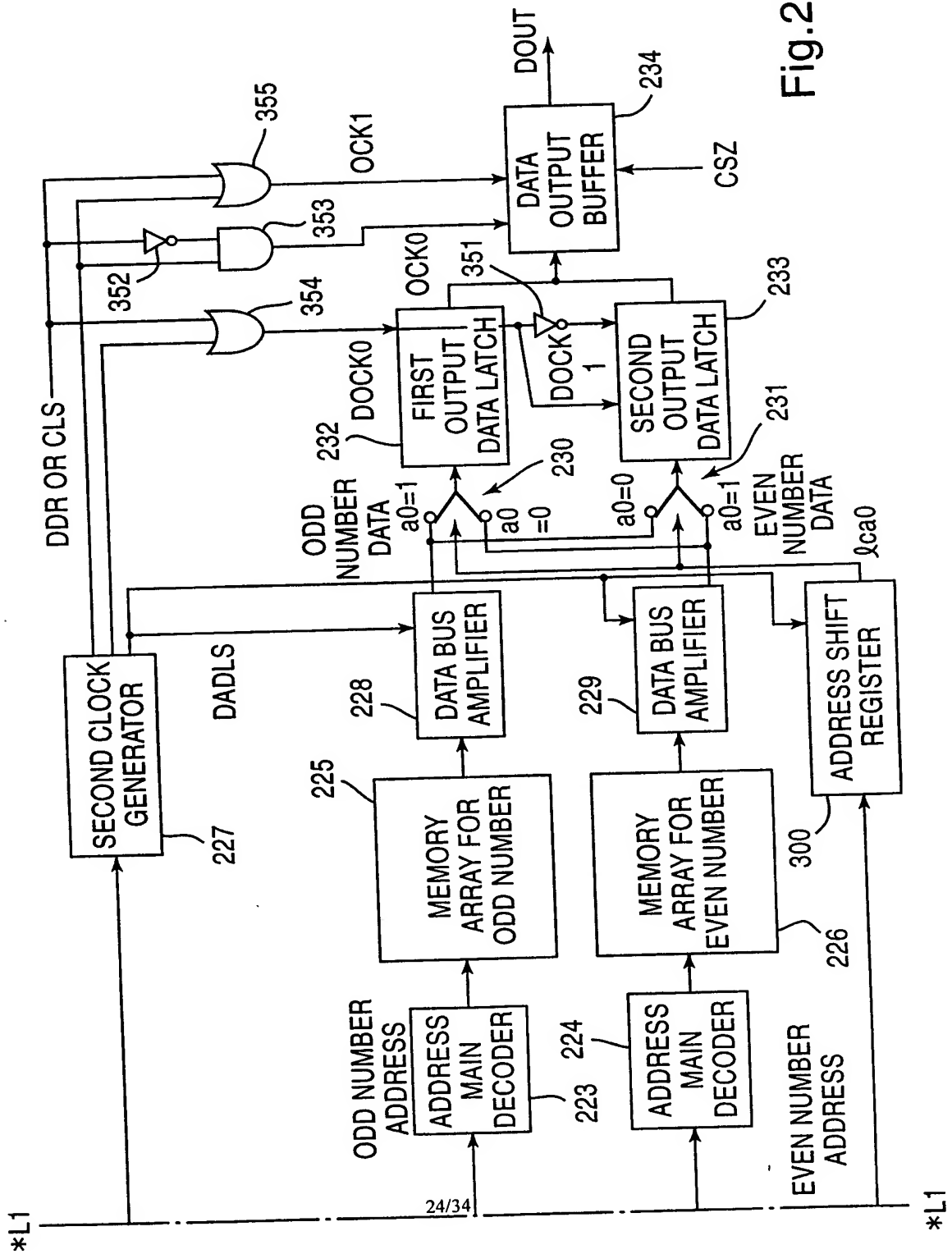


Fig.24

Fig.25

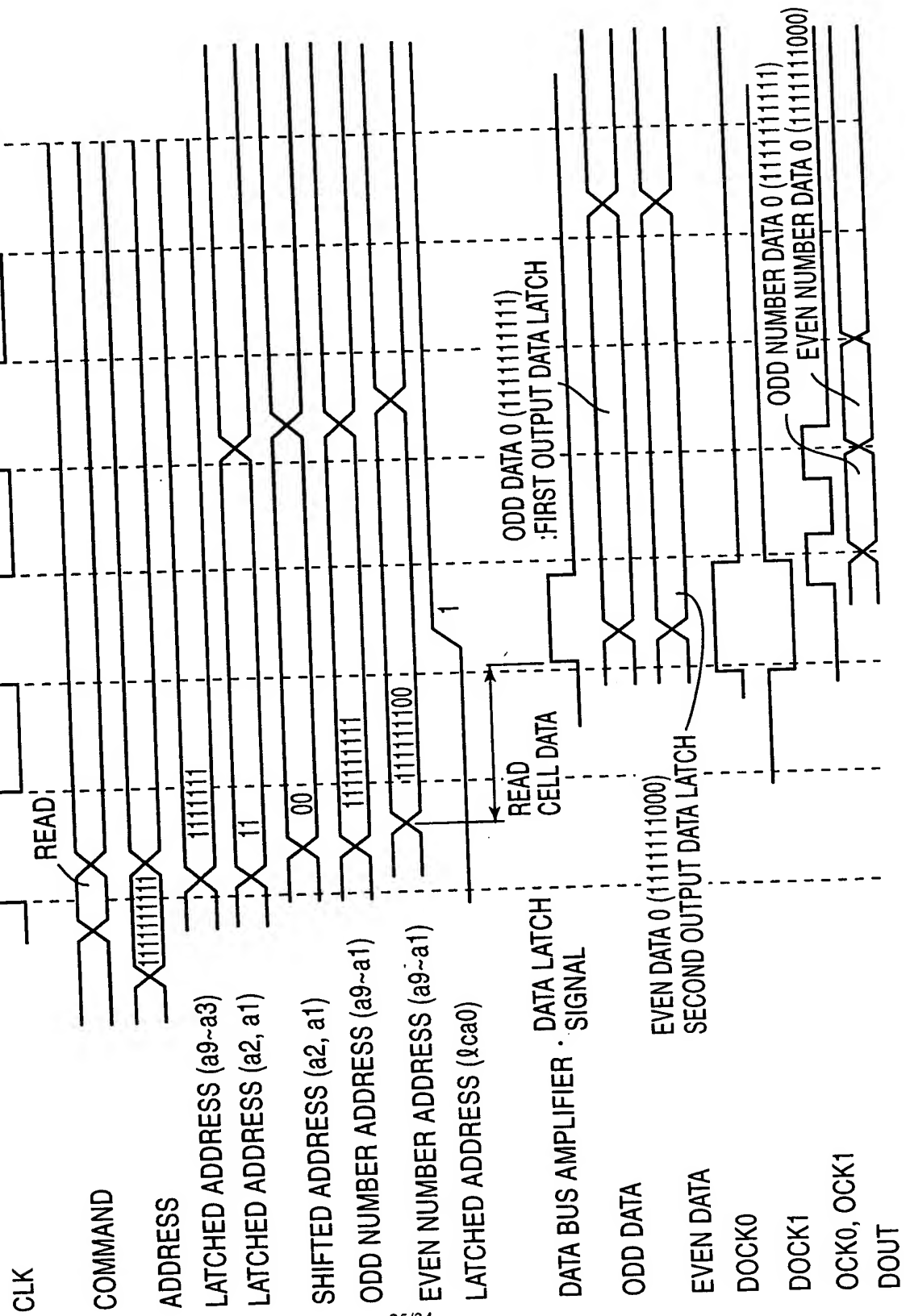


Fig. 26

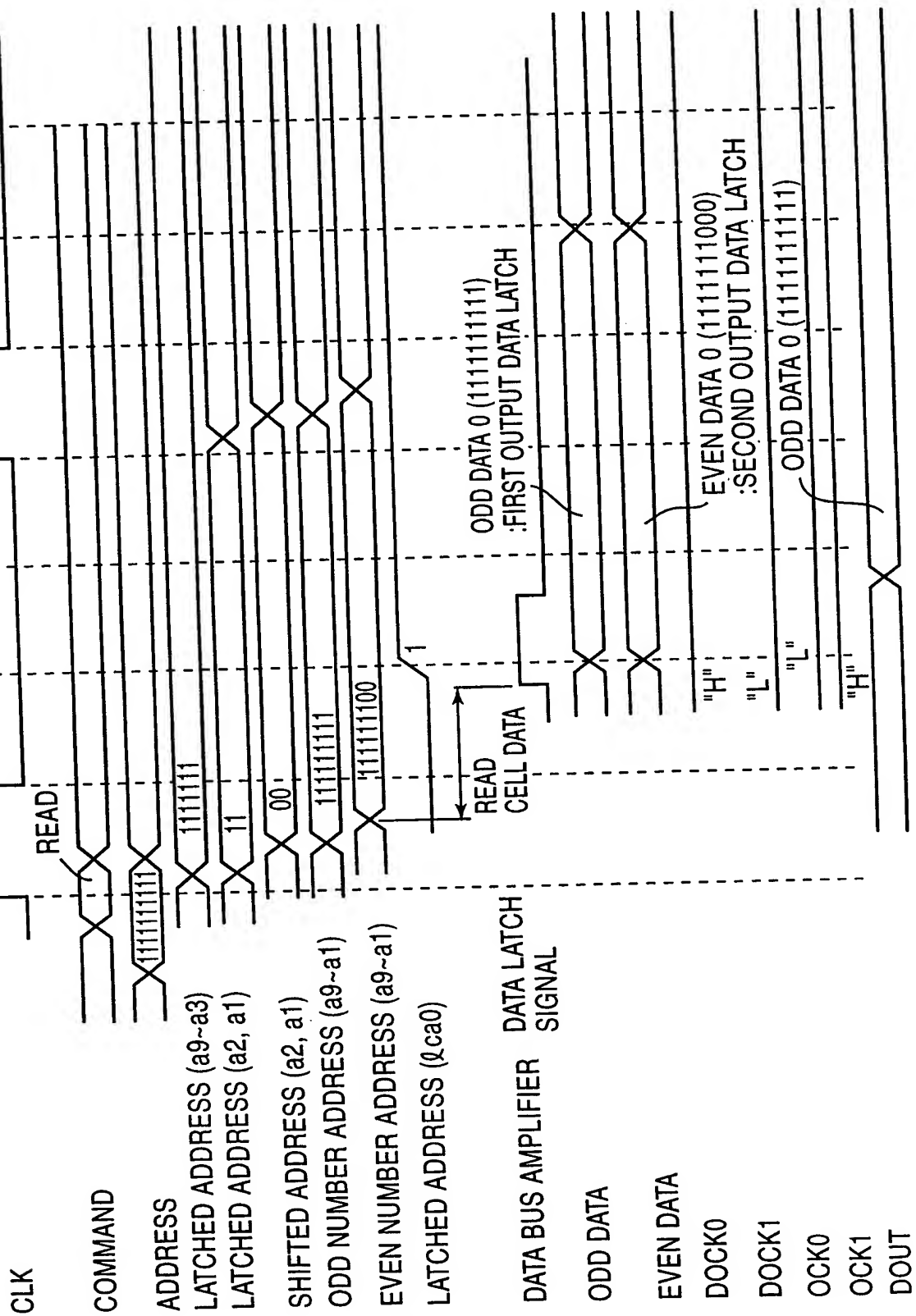
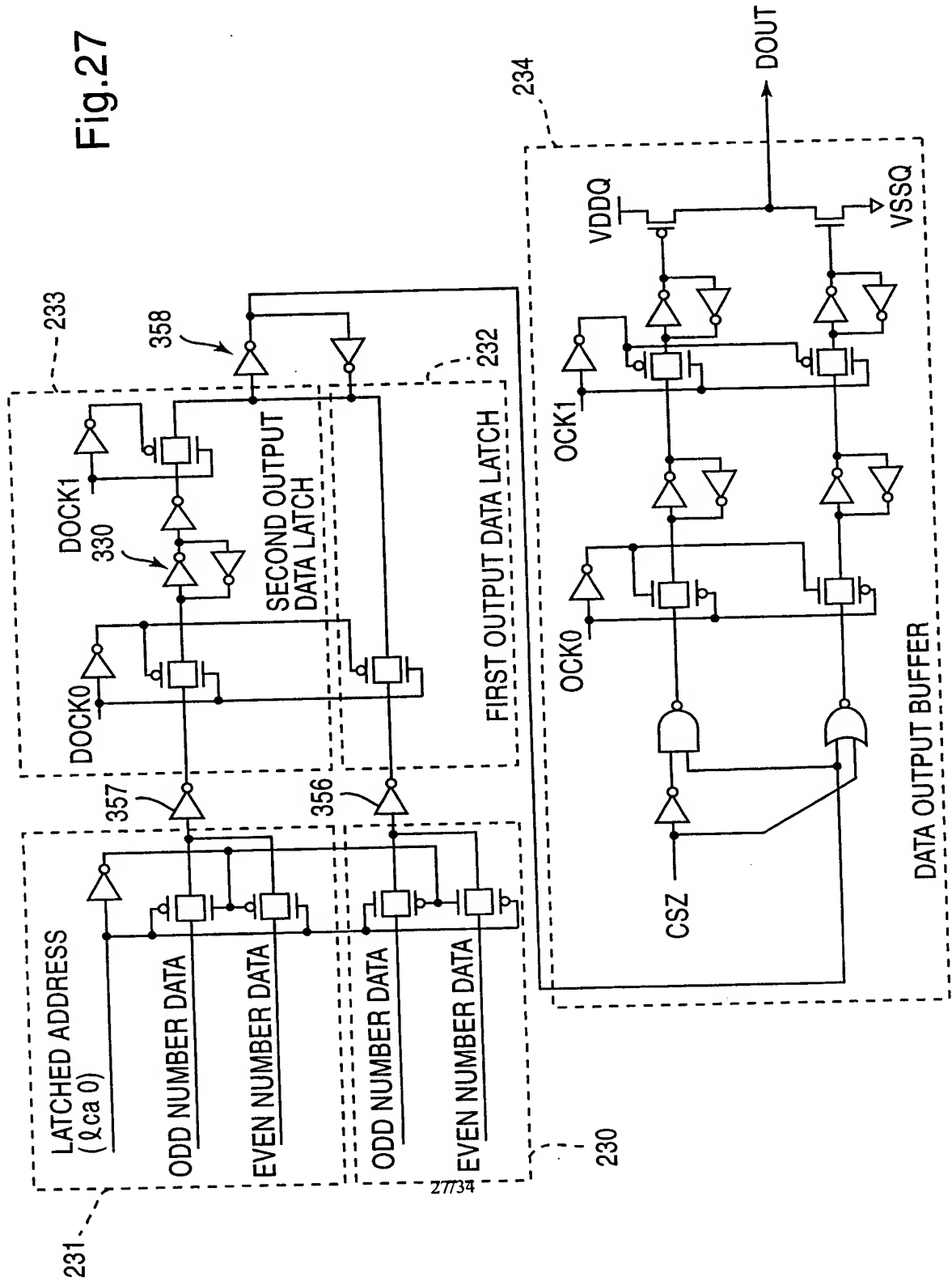


Fig.27



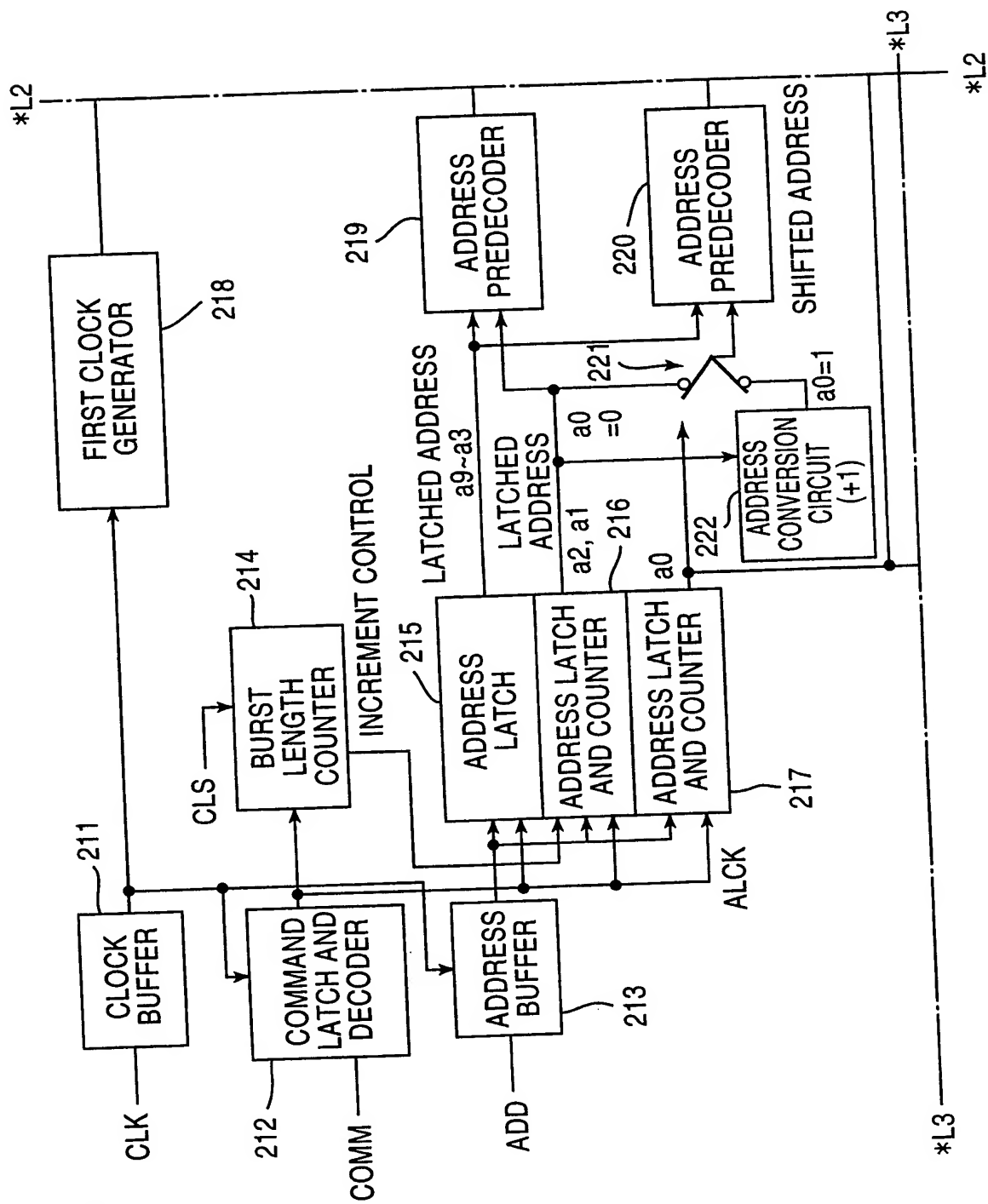


Fig.29

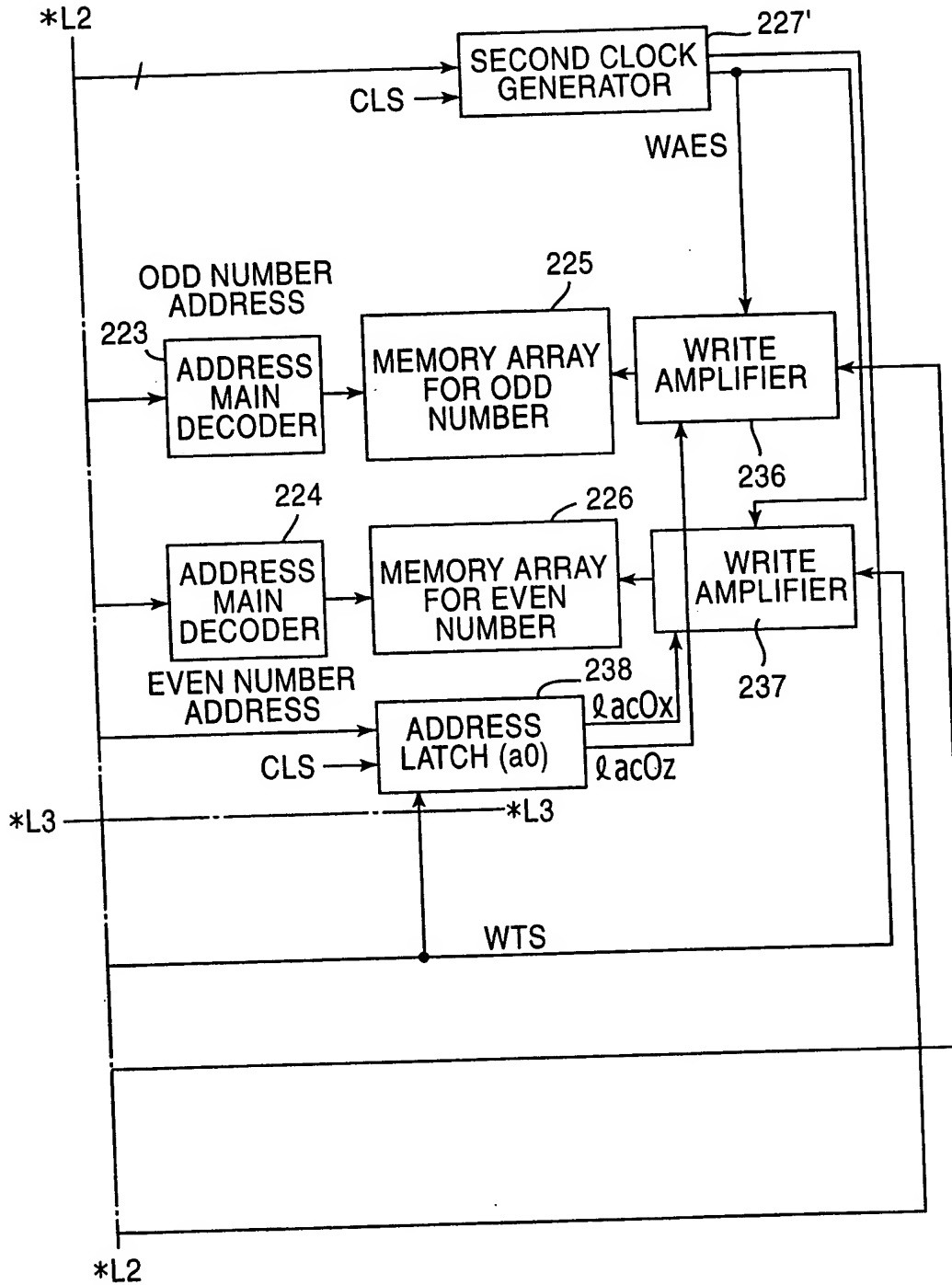


Fig.30

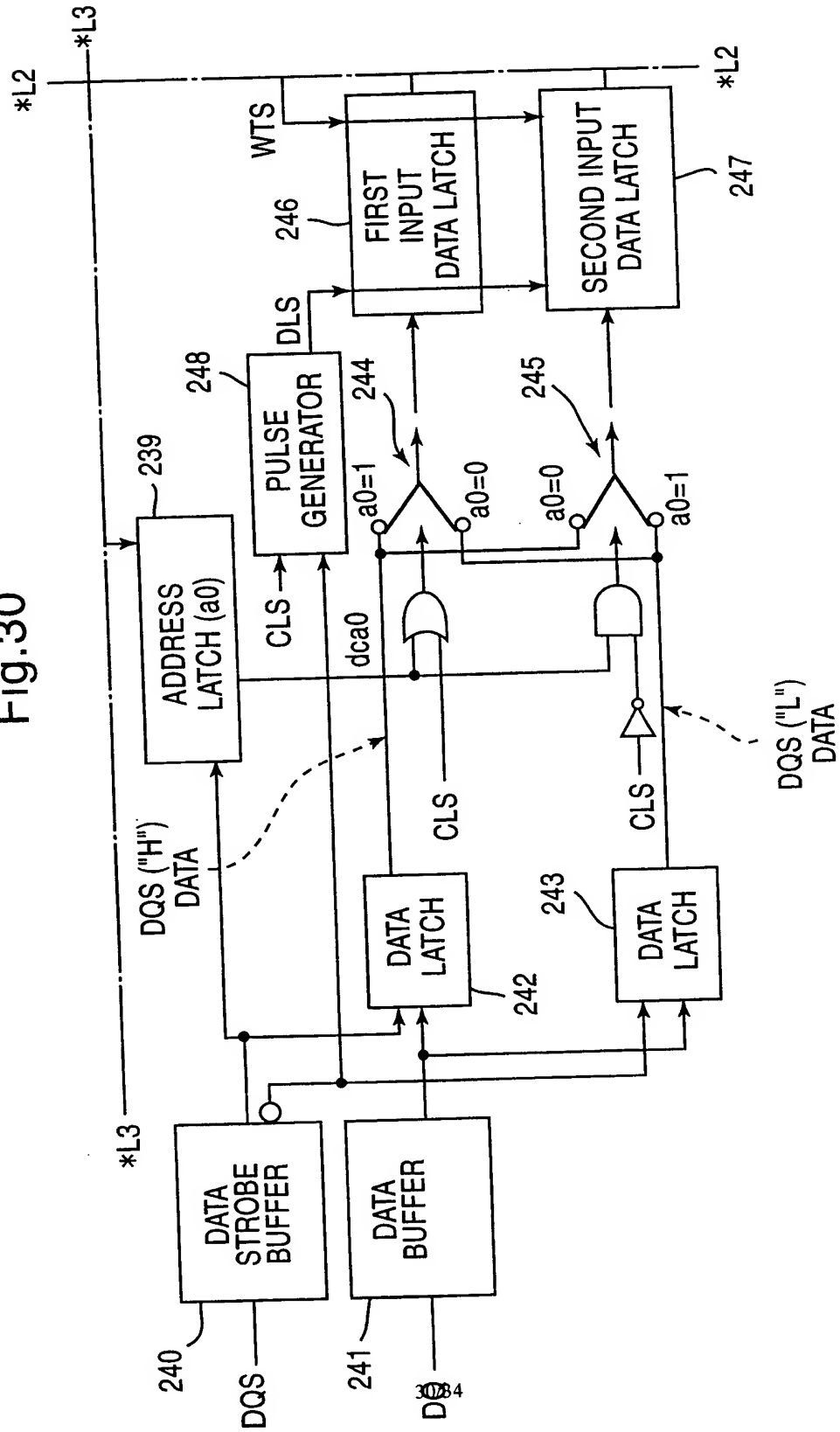


Fig.31

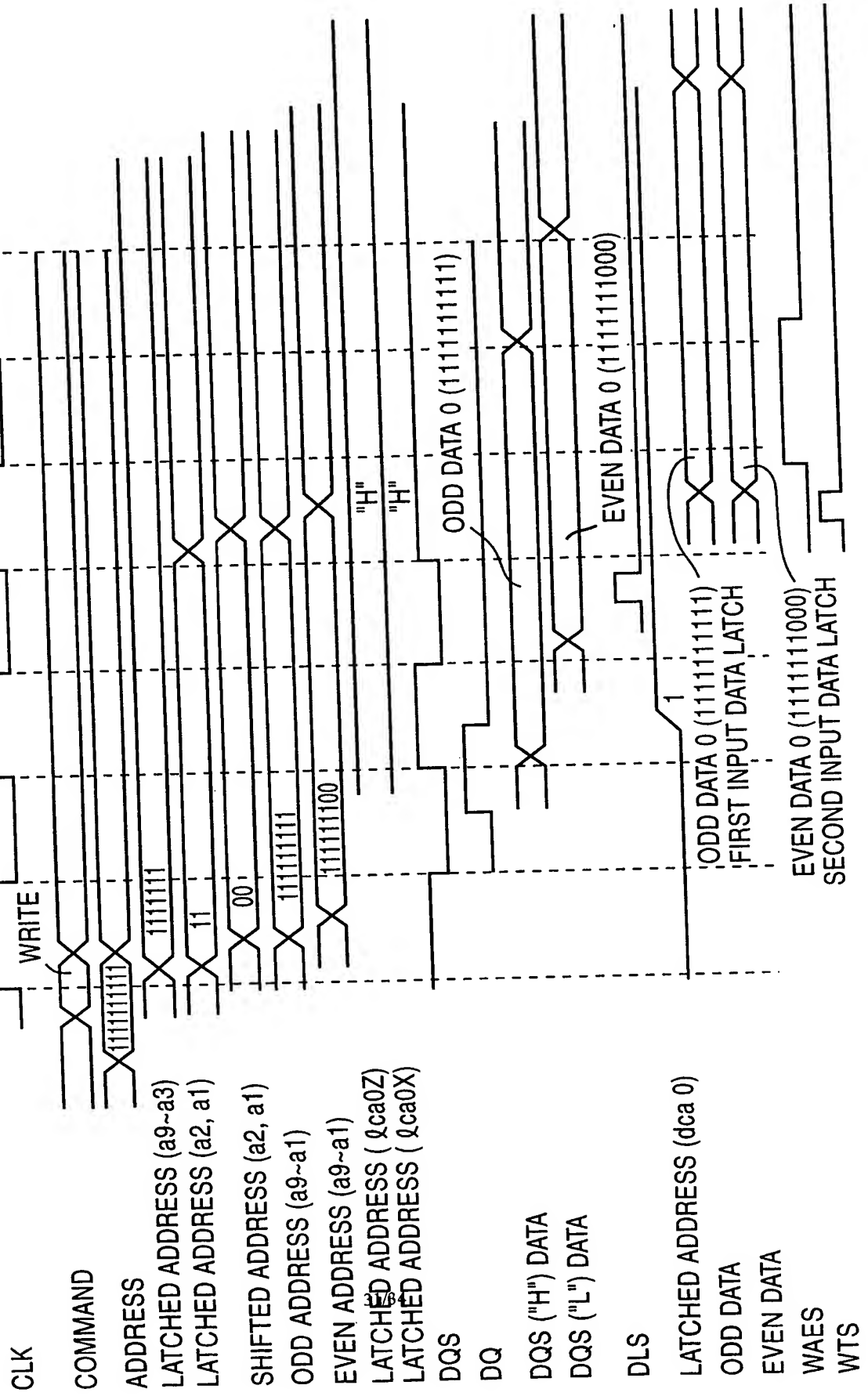


Fig.32

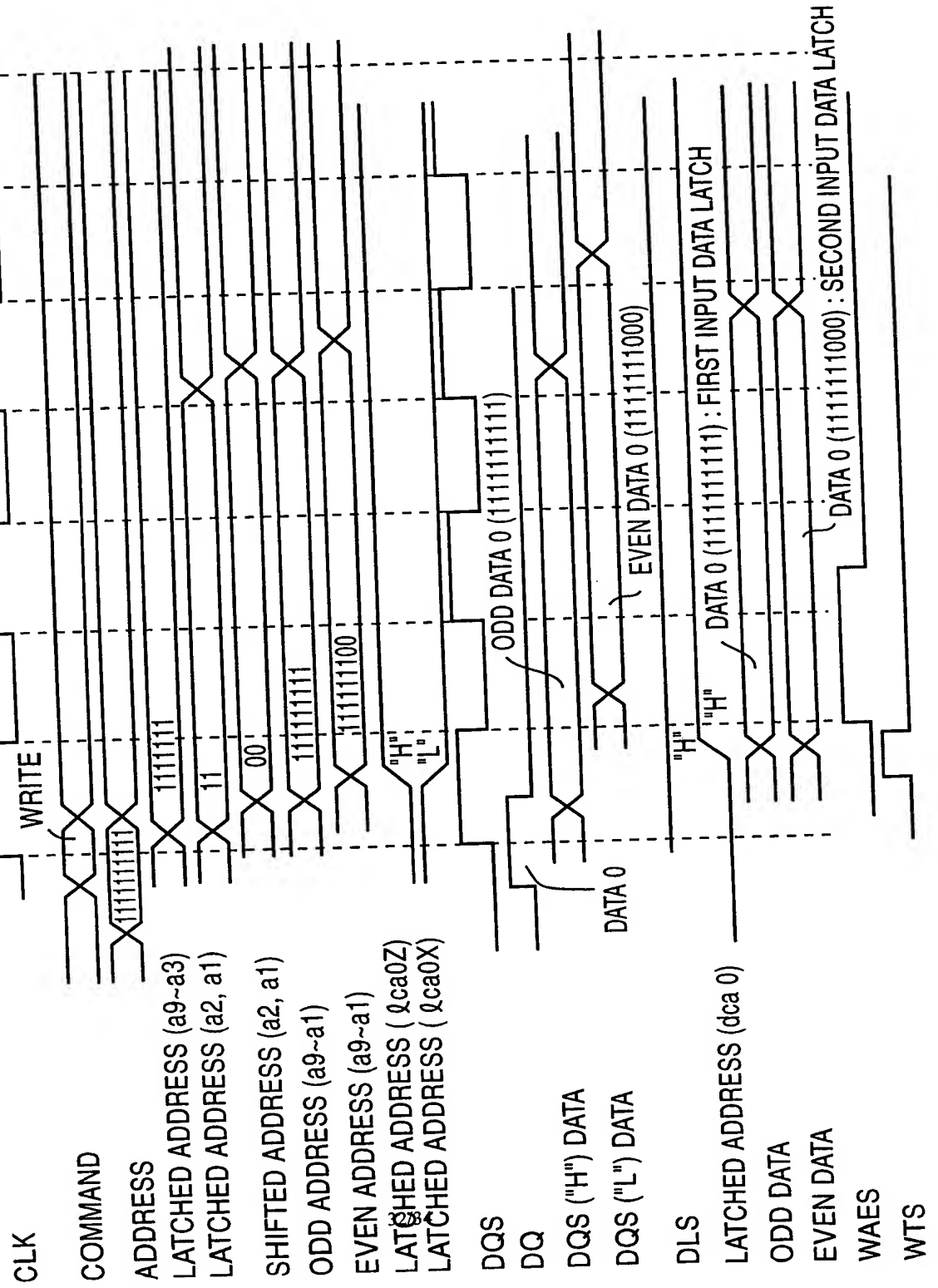
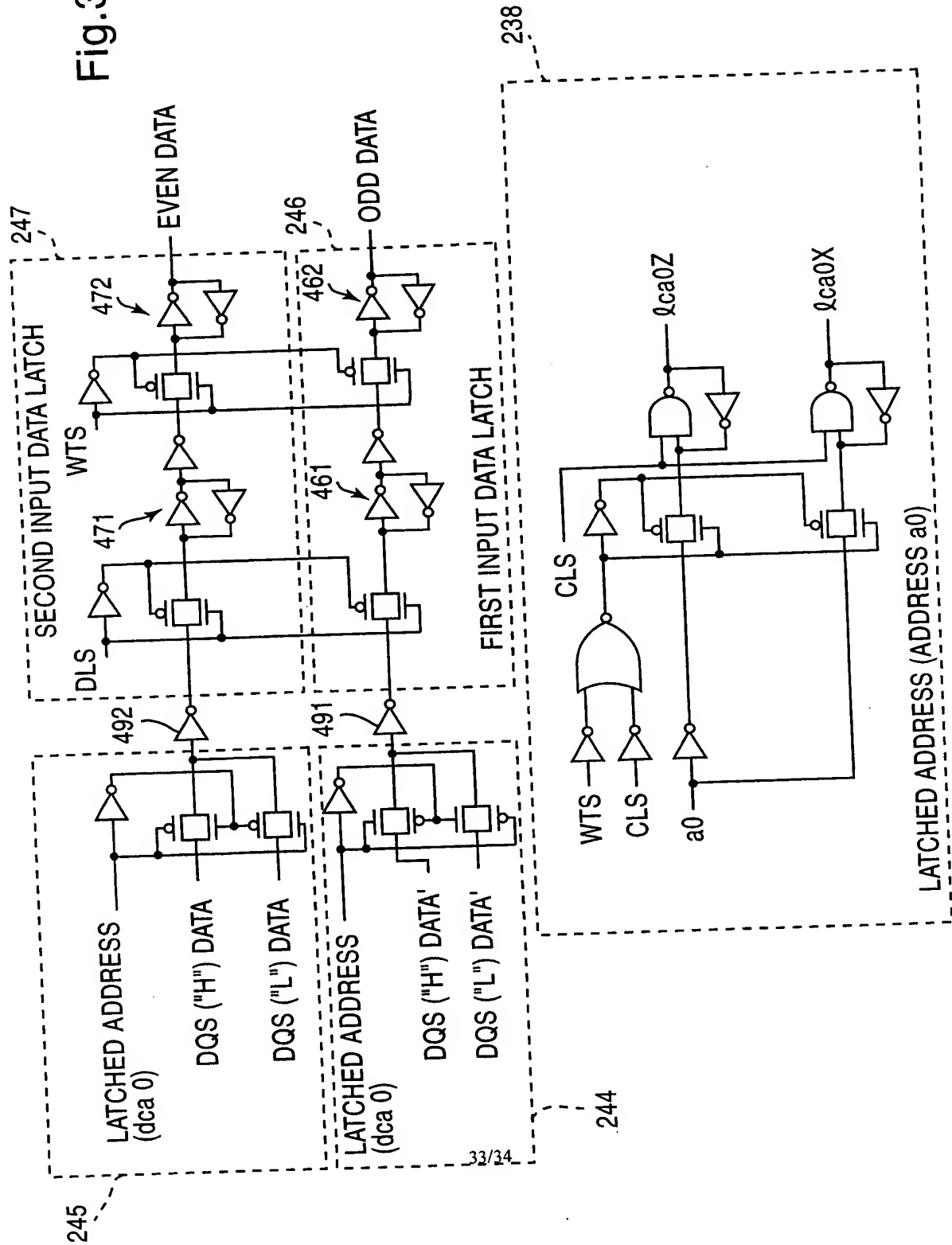


Fig.33



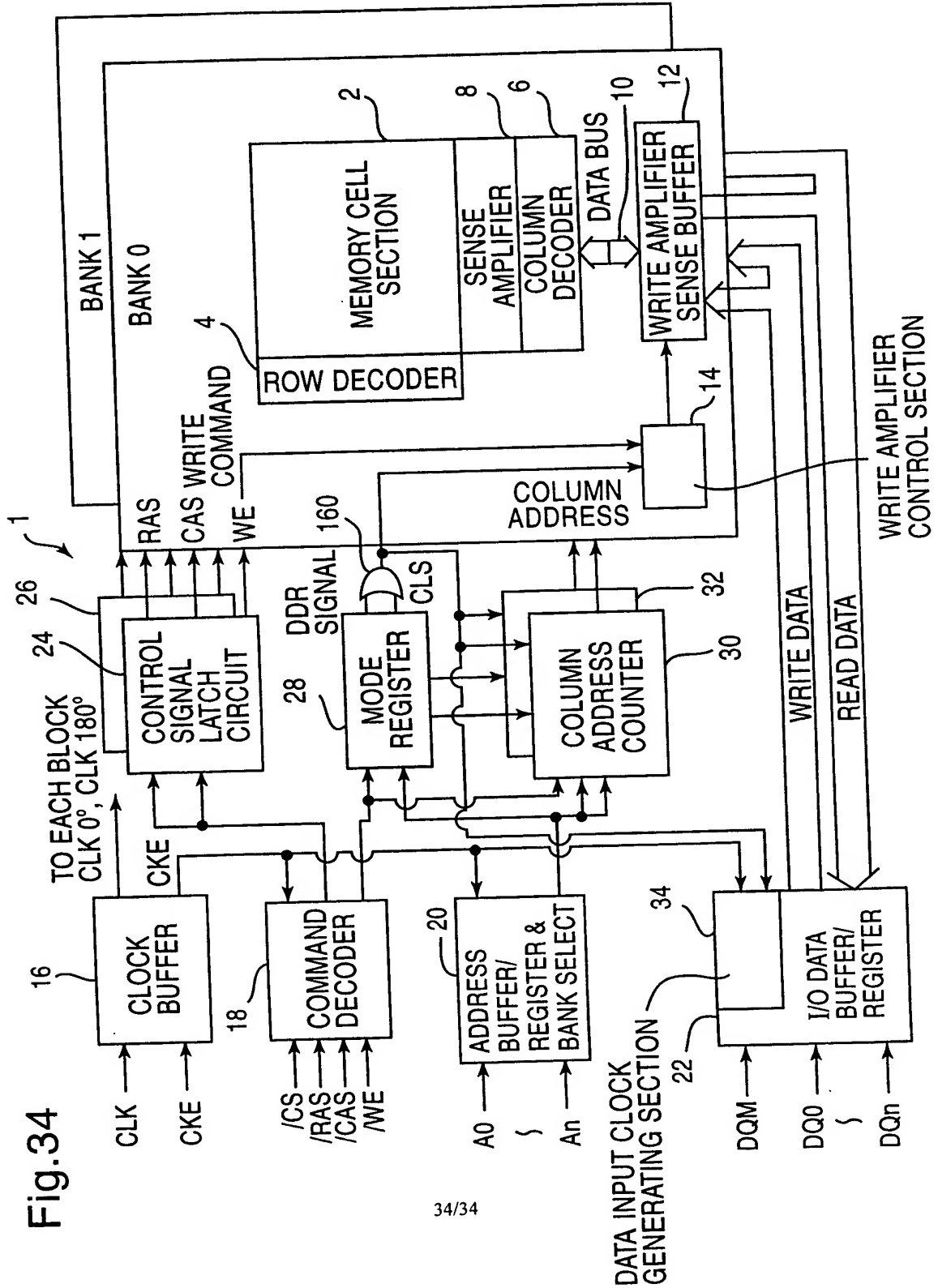


Fig.34